DATA SHEET

SAA7111A
Enhanced Video Input Processor (EVIP)

Preliminary specification
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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Four analog inputs, internal analog source selectors, e.g. 4 × CVBS or 2 × Y/C or (1 × Y/C and 2 × CVBS)
- Two analog preprocessing channels
- Fully programmable static gain for the main channels or automatic gain control for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 8-bit video CMOS analog-to-digital converters
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal-sync processing and clock generation
- Requires only one crystal (24.576 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43, NTSC-Japan and SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Real time status information output (RTCO)
- Brightness Contrast Saturation (BCS) control on-chip
- The YUV (CCIR-601) bus supports a data rate of:
  - $864 \times f_H$ = 13.5 MHz for 625 line sources
  - $858 \times f_H$ = 13.5 MHz for 525 line sources
- Data output streams for 16, 12 or 8-bit width with the following formats:
  - YUV 4 : 1 : 1 (12-bit)
  - YUV 4 : 2 : 2 (16-bit)
  - YUV 4 : 2 : 2 (CCIR-656) (8-bit)
  - RGB (5, 6, 5) (16-bit) with dither
  - RGB (8, 8, 8) (24-bit) with special application
- Odd/even field identification by a non interlace CVBS input signal
- Fix level for RGB output format during horizontal blanking
- 720 active samples per line on the YUV bus
- One user programmable general purpose switch on an output pin
- Built-in line-21 text slicer
- A 27 MHz Vertical Blanking Interval (VBI) data bypass programmable by I²C-bus for INTERCAST applications
- Power-on control
- Two via I²C-bus switchable outputs for the digitized CVBS or Y/C input signals AD1 (7 to 0) and AD2 (7 to 0)
- Chip enable function (reset for the clock generator)
- Compatible with memory-based features (line-locked clock)
- Boundary scan test circuit complies with the *IEEE Std. 1149.1 – 1990* (ID-Code = 0 F111 02 B)
- I²C-bus controlled (full read-back ability by an external controller)
- Low power (<0.5 W), low voltage (3.3 V), small package (LQFP64)
- 5 V tolerant digital I/O ports.

2 APPLICATIONS

- Desktop/Notebook (PCMCIA) video
- Multimedia
- Digital television
- Image processing
- Video phone
- Intercast.

3 GENERAL DESCRIPTION

The Enhanced Video Input Processor (EVIP) is a combination of a two-channel analog preprocessing circuit including source selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multi-standard decoder (PAL BGHI, PAL M, PAL N, NTSC M, NTSC-Japan NTSC N and SECAM), a brightness/contrast/saturation control circuit, a colour space matrix (see Fig.1) and a 27 MHz VBI-data bypass.

The pure 3.3 V CMOS circuit SAA7111A, analog front-end and digital video decoder, is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into CCIR-601 compatible colour component values. The SAA7111A accepts as analog inputs CVBS or S-video (Y/C) from TV or VTR sources. The circuit is I^2C-bus controlled.

The SAA7111A then supports several text features as Line 21 data slicing and a high-speed VBI data bypass for Intercast.

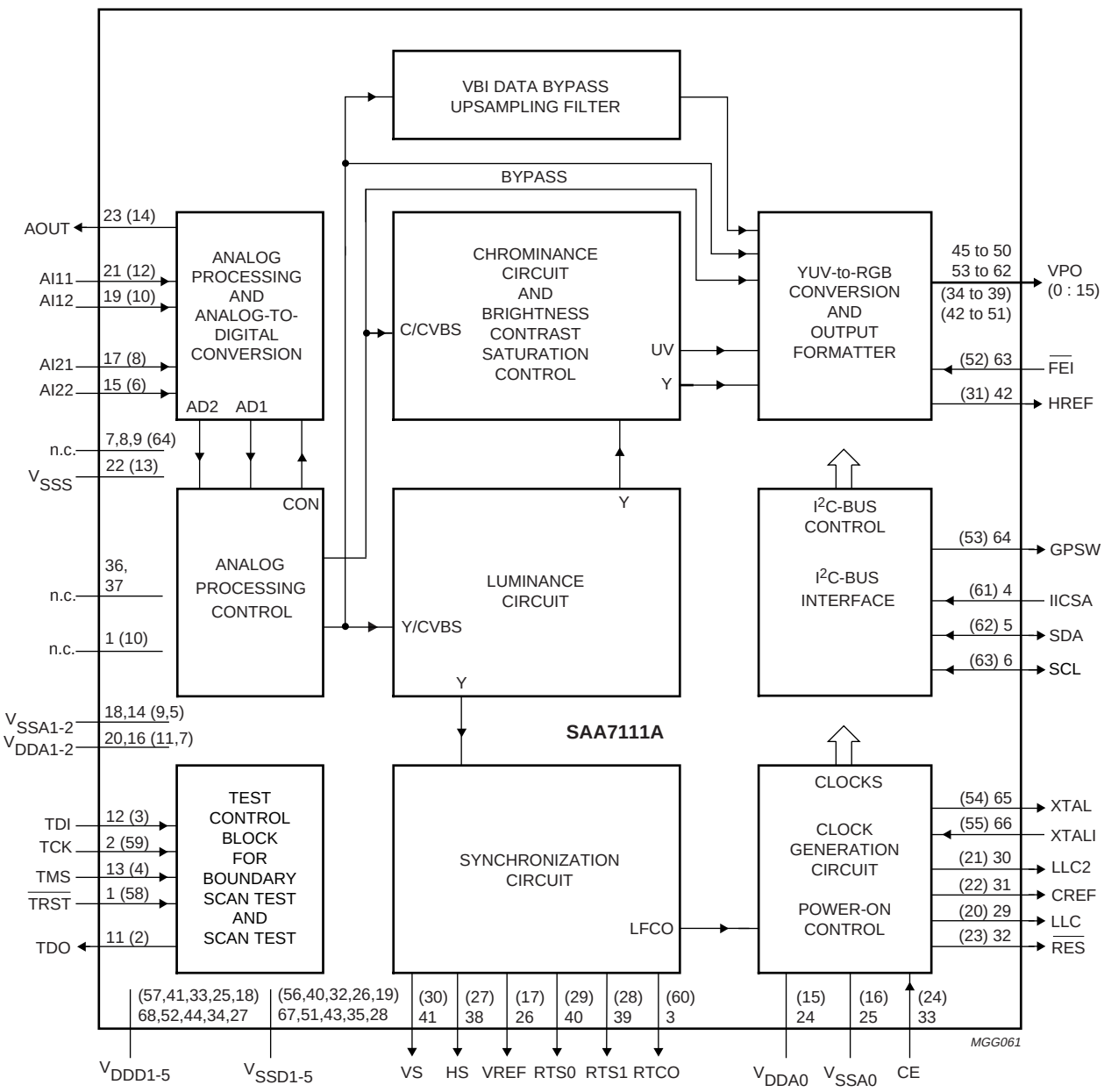
4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
T_{amb}	operating ambient temperature	0	25	70	°C
P_{A+D}	analog and digital power	–	0.5	–	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7111AHZ	LQFP64	plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm	SOT314-2
SAA7111AH	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body $14 \times 14 \times 2.7$ mm	SOT393-1
SAA7111AWP	PLCC68	plastic leaded chip carrier; 68 leads; body $24 \times 24 \times 4.5$ mm	SOT188-2

6 BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the 64-pin package.

Fig.1 Block diagram.

7 PINNING

SYMBOL	PINS		I/O/P	DESCRIPTION
	(L)QFP64	PLCC68		
n.c.	1	10	–	do not connect
TDO	2	11	O	test data output for boundary scan test; note 3
TDI	3	12	I	test data input for boundary scan test; note 3
TMS	4	13	I	test mode select input for boundary scan test or scan test; note 3
V_{SSA2}	5	14	P	ground for analog supply voltage channel 2
AI22	6	15	I	analog input 22
V_{DDA2}	7	16	P	positive supply voltage for analog channel 2 (+3.3 V)
AI21	8	17	I	analog input 21
V_{SSA1}	9	18	P	ground for analog supply voltage channel 1
AI12	10	19	I	analog input 12
V_{DDA1}	11	20	P	positive supply voltage for analog channel 1 (+3.3 V)
AI11	12	21	I	analog input 11
V_{SSS}	13	22	P	substrate ground connection
AOUT	14	23	O	analog test output; for testing the analog input channels
V_{DDA0}	15	24	P	positive supply voltage for internal Clock Generator Circuit (CGC) (+3.3 V)
V_{SSA0}	16	25	P	ground for internal CGC
VREF	17	26	O	vertical reference output signal (I^2C-bit COMPO = 0) or inverse composite blanking signal (I^2C-bit COMPO = 1) (enabled via I^2C-bus bit OEHV)
V_{DDD5}	18	27	P	digital supply voltage 5 (+3.3 V)
V_{SSD5}	19	28	P	ground for digital supply voltage 5
LLC	20	29	O	line-locked system clock output (27 MHz)
LLC2	21	30	O	line-locked clock ½ output (13.5 MHz)
CREF	22	31	O	clock reference output: this is a clock qualifier signal distributed by the internal CGC for a data rate of LLC2. Using CREF all interfaces on the VPO bus are able to generate a bus timing with identical phase. If CCIR 656 format is selected (OFTS0 = 1 and OFTS1 = 1) an inverse composite blanking signal (pixel qualifier) is provided on this pin.
$\overline{RES}$	23	32	O	reset output (active LOW); sets the device into a defined state. All data outputs are in high impedance state. The I^2C-bus is reset (waiting for start condition).
CE	24	33	I	chip enable; connection to ground forces a reset
V_{DDD4}	25	34	P	digital supply voltage input 4 (+3.3 V)
V_{SSD4}	26	35	P	ground for digital supply voltage input 4
HS	27	38	O	horizontal sync output signal (programmable); the positions of the positive and negative slopes are programmable in 8 LLC increments over a complete line (= 64 μs) via I^2C-bus bytes HSB and HSS. Fine position adjustment in 2 LLC increments can be performed via I^2C-bus bits HDEL1 and HDEL0.

SYMBOL	PINS		I/O/P	DESCRIPTION
	(L)QFP64	PLCC68		
RTS1	28	39	O	two functions output; controlled by I²C-bus bit RTSE1. RTSE1 = 0: PAL line identifier (LOW = PAL line); indicates the inverted and non-inverted R−Y component for PAL signals. RTSE1 = 1: H-PLL locked indicator; a high state indicates that the internal horizontal PLL has locked.
RTS0	29	40	O	two functions output; controlled by I²C-bus bit RTSE0. RTSE0 = 0: odd/even field identification (HIGH = odd field). RTSE0 = 1: vertical locked indicator; a HIGH state indicates that the internal Vertical Noise Limiter (VNL) has locked.
VS	30	41	O	vertical sync signal (enabled via I²C-bus bit OEHV); this signal indicates the vertical sync with respect to the YUV output. The HIGH period of this signal is approximately six lines if the VNL function is active. The positive slope contains the phase information for a deflection controller.
HREF	31	42	O	horizontal reference output signal (enabled via I²C-bus bit OEHV); this signal is used to indicate data on the digital YUV bus. The positive slope marks the beginning of a new active line. The HIGH period of HREF is 720 Y samples long. HREF can be used to synchronize data multiplexer/demultiplexer. HREF is also present during the vertical blanking interval.
V_{SSD3}	32	43	P	ground for digital supply voltage input 3
V_{DDD3}	33	44	P	digital supply voltage 3 (+3.3 V)
VPO (15 to 10)	34 to 39	45 to 50	O	digital VPO-bus (Video Port Out) signal; higher bits of the 16-bit VPO-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing scheme of the VPO-bus are controlled via I²C-bus bits OFTS0 and OFTS1. If I²C-bus bit VIPB = 1 the six MSBs of the digitized input signal are connected to these outputs, configured by the I²C-bus 'MODE' bits (see Figs 34 to 41): LUMA -> VPO15 to VPO8, CHROMA -> VPO7 to VPO0.
V_{SSD2}	40	51	P	ground for digital supply voltage input 2
V_{DDD2}	41	52	P	digital supply voltage 2 (+3.3 V)
VPO (9 to 0)	42 to 51	53 to 62	O	digital VPO-bus output signal; lower bits of the 16-bit YUV-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing schema of the VPO-bus are controlled via I²C-bus bits OFTS0 and OFTS1. If I²C-bus bit VIPB = 1 the digitized input signal are connected to these outputs, configured by the I²C-bus 'MODE' bits (see Figs 34 to 41): LUMA -> VPO15 to VPO8, CHROMA -> VPO7 to VPO0.
$\overline{FEI}$	52	63	I	fast enable input signal (active LOW); this signal is used to control fast switching on the digital YUV-bus. A HIGH at this input forces the IC to set its Y and UV outputs to the high impedance state.
GPSW	53	64	O	general purpose switch output; the state of this signal is set via I²C-bus control and the levels are TTL compatible
XTAL	54	65	O	second terminal of crystal oscillator; not connected if external clock signal is used
XTALI	55	66	I	input terminal for 24.576 MHz crystal oscillator or connection of external oscillator with CMOS compatible square wave clock signal
V_{SSD1}	56	67	P	ground for digital supply voltage input 1

SYMBOL	PINS		I/O/P	DESCRIPTION
	(L)QFP64	PLCC68		
V_{DDD1}	57	68	P	digital supply voltage input 1 (+3.3 V)
$\overline{TRST}$	58	1	I	test reset input not (active LOW), for boundary scan test; notes 1, 2 and 3
TCK	59	2	I	test clock for boundary scan test; note 3
RTCO	60	3	O	real time control output: contains information about actual system clock frequency, subcarrier frequency and phase and PAL sequence
IICSA	61	4	I	I^2C-bus slave address select; 0 = 48H for write, 49H for read 1 = 4AH for write, 4BH for read
SDA	62	5	I/O	serial data input/output (I^2C-bus)
SCL	63	6	I/O	serial clock input/output (I^2C-bus)
n.c.	64	7, 8, 9, 36 and 37	–	do not connect

Notes

1. For board design without boundary scan implementation (pin compatibility with the SAA7110) connect the $\overline{TRST}$ pin to ground.
2. This pin provides easy initialization of BST circuit. $\overline{TRST}$ can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once.
3. In accordance with the *IEEE1149.1* standard the pads TCK, TDI, TMS and $\overline{TRST}$ are input pads with an internal pull-up transistor and TDO a 3-state output pad.

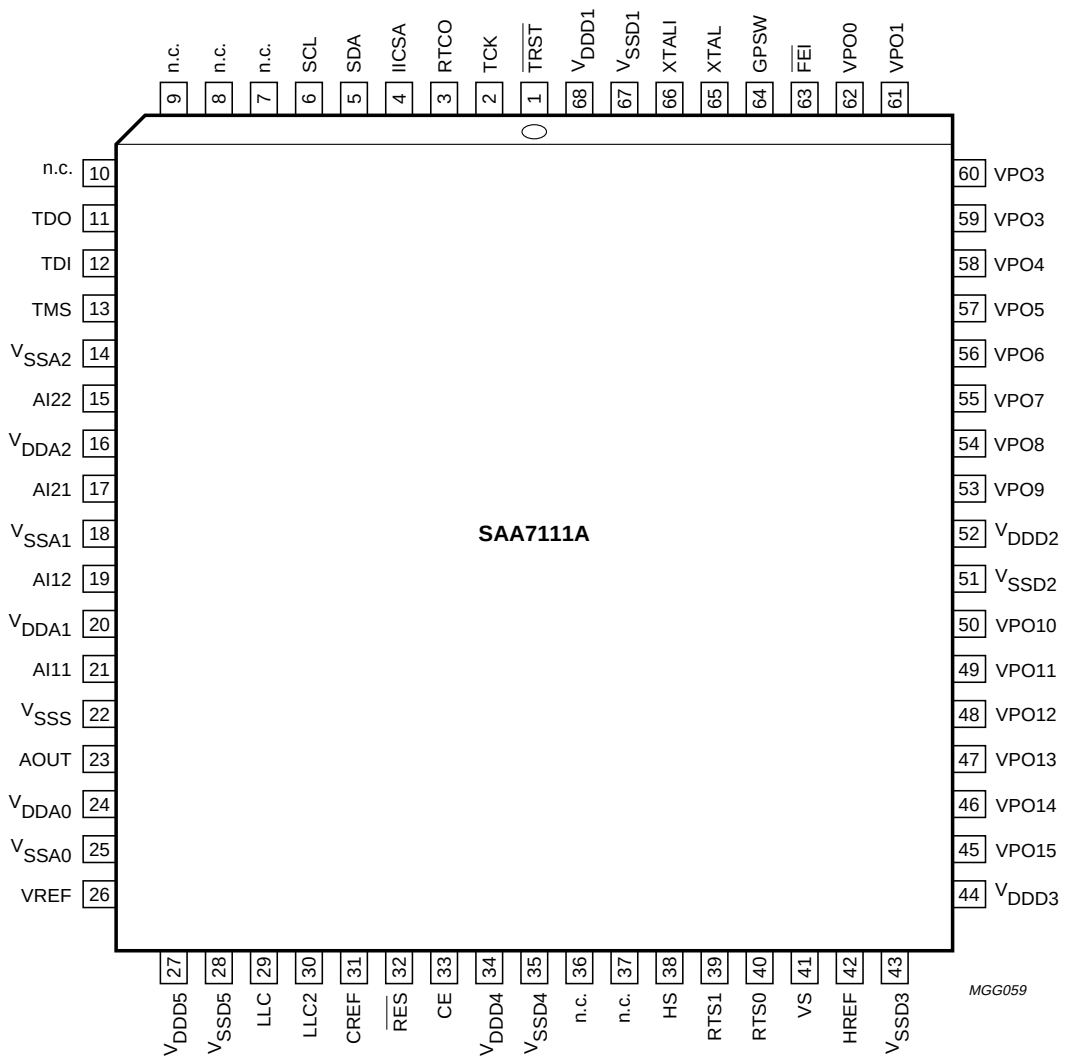


Fig.2 Pin configuration (PLCC68).

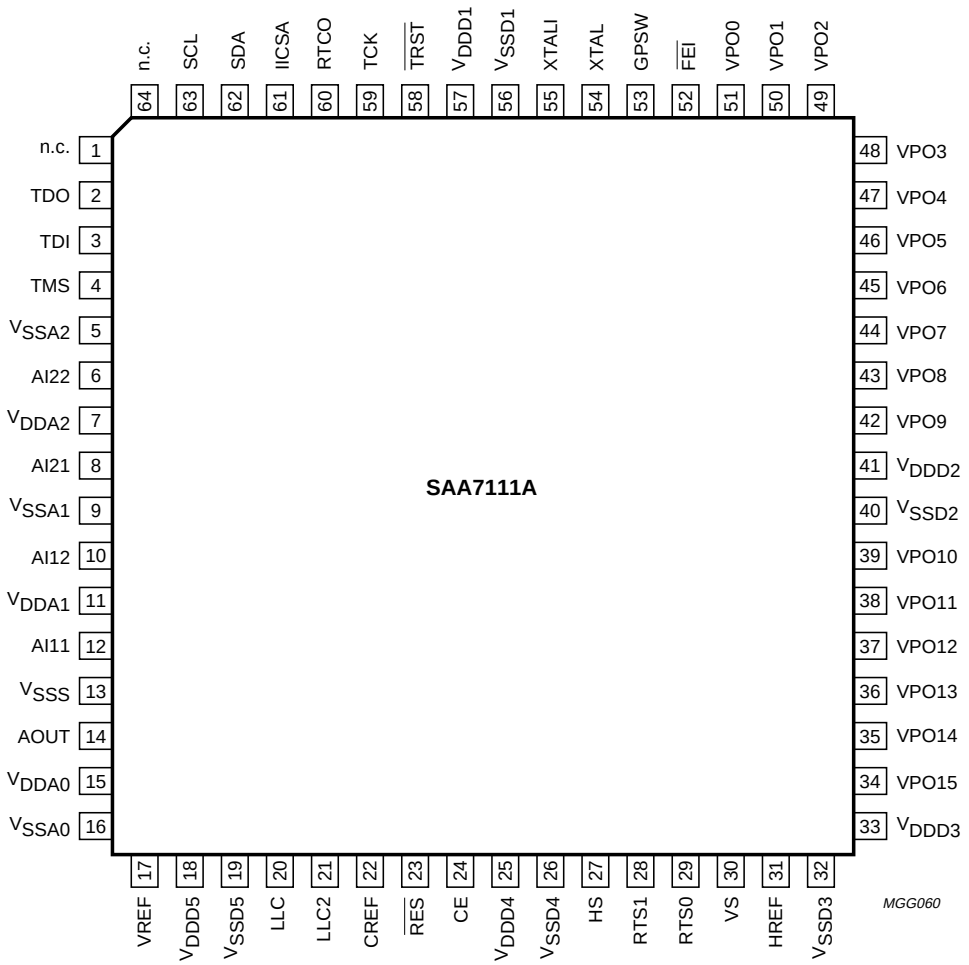


Fig.3 Pin configuration (LQFP64/QFP64).

8 FUNCTIONAL DESCRIPTION

8.1 Analog input processing

The SAA7111A offers four analog signal inputs, two analog main channels with source switch, clamp circuit, analog amplifier, anti-alias filter and video CMOS ADC (see Fig.6).

8.2 Analog control circuits

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. During the vertical blanking time, gain and clamping control are frozen.

8.2.1 CLAMPING

The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal.

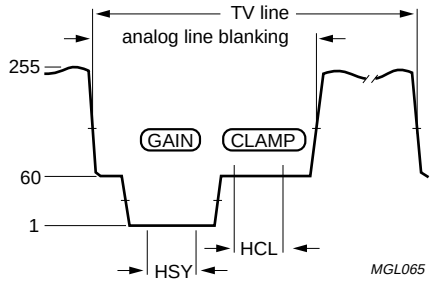


Fig.4 Analog line with clamp (HCL) and gain range (HSY).

8.2.2 GAIN CONTROL

Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figs 14 and 15) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

The gain control circuit receives (via the I^2C-bus) the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built-in automatic gain control (AGC) as part of the Analog Input Control (AICO).

The AGC (automatic gain control for luminance) is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal.

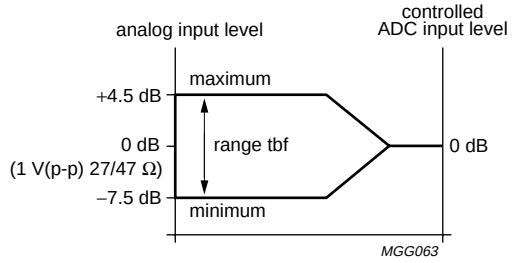


Fig.5 Automatic gain range.

8.3 Chrominance processing

The 8-bit chrominance signal is fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator DTO1 are applied (0 and 90° phase relationship to the demodulator axis). The frequency is dependent on the present colour standard. The output signals of the multipliers are low-pass filtered (four programmable characteristics) to achieve the desired bandwidth for the colour difference signals (PAL, NTSC) or the 0 and 90° FM-signals (SECAM).

The colour difference signals are fed to the Brightness/Contrast/Saturation block (BCS), which includes the following five functions:

- AGC (Automatic Gain Control for chrominance PAL and NTSC)
- Chrominance amplitude matching (different gain factors for R−Y and B−Y to achieve CCIR-601 levels Cr and Cb for all standards)
- Chrominance saturation control
- Luminance contrast and brightness.
- Limiting YUV to the values 1 (min.) and 254 (max.) to fulfil CCIR-601 requirements.

The SECAM-processing contains the following blocks:

- Baseband 'bell' filters to reconstruct the amplitude and phase equalized 0 and 90° FM-signals
- Phase demodulator and differentiator (FM-demodulation)
- De-emphasis filter to compensate the pre-emphasised input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM-switch signal).

The burst processing block provides the feedback loop of the chroma PLL and contains;

- Burst gate accumulator
- Colour identification and killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)
- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, H/2-switch generation
- Increment generation for DTO1 with divider to generate stable subcarrier for non-standard signals.

The chrominance comb filter block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC colour standards the chrominance comb filter can be used to eliminate crosstalk from luminance to chrominance (cross-colour) for vertical structures. The comb filter can be switched off if desired. The embedded line delay is also used for SECAM recombination (cross-over switches).

The resulting signals are fed to the variable Y-delay compensation, RGB matrix, dithering circuit and output interface, which contains the VPO output formatter and the output control logic (see Fig.7).

8.4 Luminance processing

The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_0 = 4.43 or 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be bypassed for S-video (S-VHS, HI8) signals.

The high frequency components of the luminance signal can be peaked (control for sharpness improvement via I^2C-bus) in two band-pass filters with selectable transfer characteristic. This signal is then added to the original (unpeaked) signal. A switchable amplifier achieves common DC amplification, because the DC gains are different in both chrominance trap modes. The improved luminance signal is fed to the BCS control located in the chrominance processing block (see Fig.8).

8.5 RGB matrix

Y, Cr and Cb data are converted after interpolation into RGB data in accordance with CCIR-601 recommendations. The realized matrix equations consider the digital quantization:

$$R = Y + 1.371\ Cr$$

$$G = Y - 0.336\ Cb - 0.698\ Cr$$

$$B = Y + 1.732\ Cb$$

After dithering (noise shaping) the RGB data is fed to the output interface within the VPO-bus output formatter.

8.6 VBI-data bypass

For a 27 MHz VBI-data bypass the offset binary CVBS signal is upsampled behind the ADCs. Upsampling of the CVBS signal from 13.5 to 27 MHz is possible, because the ADCs deliver high performance at 13.5 MHz sample clock. Suppressing of the back folded CVBS frequency components after upsampling is achieved by an interpolation filter (see Fig.43).

The TUF block on the digital top level performs the upsampling and interpolation for the bypassed CVBS signal (see Fig.7).

For bypass details see Figs 9 to 11.

8.7 VPO-bus (digital outputs)

The 16-bit VPO-bus transfers digital data from the output interfaces to a feature box or a field memory, a digital colour space converter (SAA7192 DCSC), a video enhancement and digital-to-analog processor (SAA7165 VEDA2) or a colour graphics board (Targa-format) as a graphical user interface.

The output data formats are controlled via the I²C-bus bits OFTS0, OFTS1 and RGB888. Timing for the data stream formats, YUV (4,: 1 : 1) (12-bit), YUV (4,: 2 : 2) (16-bit), RGB (5, 6, 5) (16-bit) and RGB (8, 8, 8) (24-bit) with an LLC2 data rate, is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference) (except RGB (8, 8, 8), see special application in Fig.33).
The higher output signals VPO15 to VPO8 in the YUV format perform the digital luminance signal. The lower output signals VPO7 to VPO0 in the YUV format are the bits of the multiplexed colour difference signals (B–Y) and (R–Y). The arrangement of the RGB (5, 6, 5) and RGB (8, 8, 8) data stream bits on the VPO-bus is given in Table 6.

The data stream format YUV 4 : 2 : 2 (the 8 higher output signals VPO15 to VPO8) in LLC data rate fulfils the CCIR-656 standard with its own timing reference code at the start and end of each video data block.

A pixel in the format tables is the time required to transfer a full set of samples. If 16-bit 4 : 2 : 2 format is selected two luminance samples are transmitted in comparison to one (B–Y) and one (R–Y) sample within a pixel.The time frames are controlled by the HREF signal.

Fast enable is achieved by setting input $\overline{FEI}$ to LOW. The signal is used to control fast switching on the digital VPO-bus. HIGH on this pin forces the VPO outputs to a high-impedance state (see Figs 19 and 20). The I²C-bus bit OEYC has to be set HIGH to use this function.

The digitized PAL, SECAM or NTSC signals AD1 (7 to 0) and AD2 (7 to 0) are connected directly to the VPO-bus via I²C-bus bit VIPB = 1 and MODE = 4, 5, 6 or 7.

AD1 (7 to 0) -> VPO (15 to 8) and
AD2 (7 to 0) -> VPO (7 to 0)

The selection of the analog input channels is controlled via I²C-bus subaddress 02 MODE select.

The upsampled 8-bit offset binary CVBS signal (VBI-data bypass) is multiplexed under control of the I²C-bus to the digital VPO-bus (see Fig.9).

8.8 Reference signals HREF, VREF and CREF

- HREF: The positive slope of the HREF output signal indicates the beginning of a new active video line. The high period is 720 luminance samples long and is also present during the vertical blanking.
  The description of timing and position from HREF is illustrated in Figs 16, 17, 22 and 24.
- VREF: The VREF output delivers a vertical reference signal or an inverse composite blank signal controlled via the I²C-bus [subaddress 11, inverse composite blank (COMPO)]. Furthermore four different modes of vertical reference signals are selectable via the I²C-bus [subaddress 13, vertical reference output control (VCTR1 and VCTR0)]. The description of VREF timing and position is illustrated in Figs 16, 17, 25 and 26.
- CREF: The CREF output delivers a clock/pixel qualifier signal for external interfaces to synchronize to the VPO-bus data stream.

  Four different modes for the clock qualifier signal are selectable via the I²C-bus [subaddress 13, clock reference output control (CCTR1 and CCTR0]. The description of CREF timing and position is illustrated in Figs 17, 19, 21 and 22.

8.9 Synchronization

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e. g. HCL and HSY) are generated in accordance with analog front-end requirements. The output signals HS, VS, and PLIN are locked to the timing reference, guaranteed between the input signal and the HREF signal, as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications which require absolute timing accuracy on the input signals. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO (see Fig.8).

8.10 Clock generation circuit

The internal CGC generates all clock signals required for the video input processor. The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency (6.75 MHz = 429/432 $\times$ f_H). Internally the LFCO signal is multiplied by a factor of 2 or 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the LLC and LLC2 output clock signals.
The rectangular output clocks have a 50% duty factor (see Fig.27).

8.11 Power-on reset and CE input

A missing clock, insufficient digital or analog V_{DDA0} supply voltages (below 2.7 V) will initiate the reset sequence; all outputs are forced to 3-state. The indicator output $\overline{RES}$ is LOW for approximately 128LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

It is possible to force a reset by pulling the chip enable (CE) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA return from 3-state to active, while HREF, VREF, HS and VS remain in 3-state and have to be activated via I²C-bus programming (see Table 5).

8.12 RTCO output

The real time control and status output signal contains serial information about the actual system clock (increment of the HPLL), subcarrier frequency [increment and phase (via reset) of the FSC-PLL] and PAL sequence bit. The signal can be used for various applications in external circuits, e.g. in a digital encoder to achieve clean encoding (see Fig.21).

8.13 The Line-21 text slicer

The text slicer block detects and acquires Line-21 Closed Captioning data from a 525-line CVBS signal. Extended data services on Line-21 Field 2 are also supported.
If valid data is detected the two data bytes are stored in two I²C-bus registers. A parity check is also performed and the result is stored in the MSB of the corresponding byte.
A third I²C-bus register is provided for data valid and data ready flags. The two bits F1VAL and F2VAL indicate that the input signal carries valid Closed Captioning data in the corresponding fields. The data ready bits F1RDY and F2RDY have to be evaluated if asynchronous I²C-bus reading is used.

8.13.1 Suggestions for I²C-bus interface of the display software reading line-21 data

There are two methods by which the software can acquire the data:

1. Synchronous reading once per frame (or once per field); It can use either the rising edge (Line-21 Field 1) or both edges (Line-21 Field 1 or 2) of the ODD signal (pin RTSO) to initiate an I²C-bus read transfer of the three registers 1A, 1B and 1C.
2. Asynchronous reading; It can poll either the F1RDY bit (Line-21 Field 1) or both F1RDY/F2RDY bits (Line-21 Field 1 or 2). After valid data has been read the corresponding F*RDY bit is set to LOW until new data has arrived. The polling frequency has to be slightly higher than the frame or field frequency, respectively.

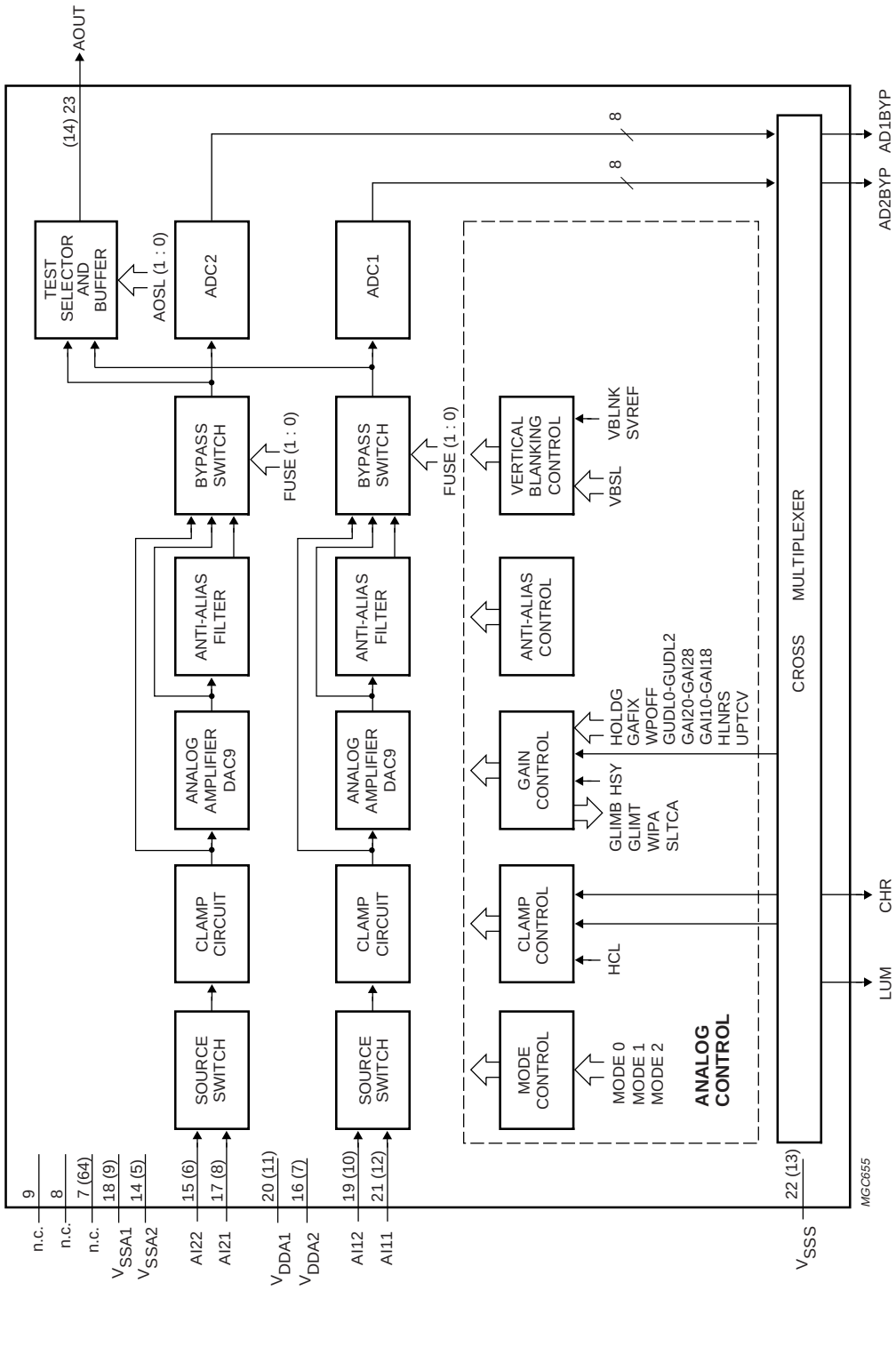


Fig.6 Analog input processing.

The pin numbers given in parenthesis refer to the 64-pin package.

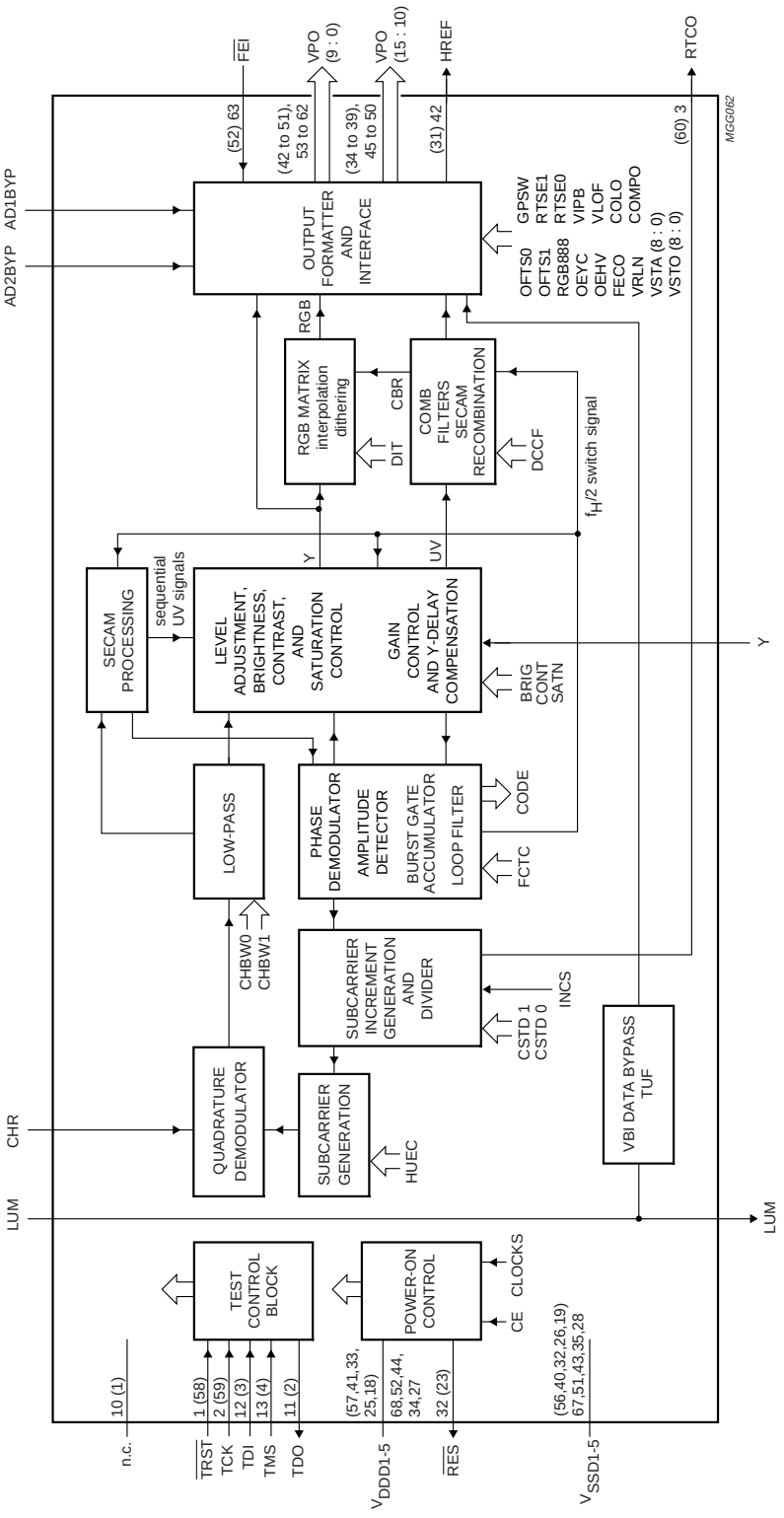


Fig.7 Chrominance circuit.

The pin numbers given in parenthesis refer to the 64-pin package.

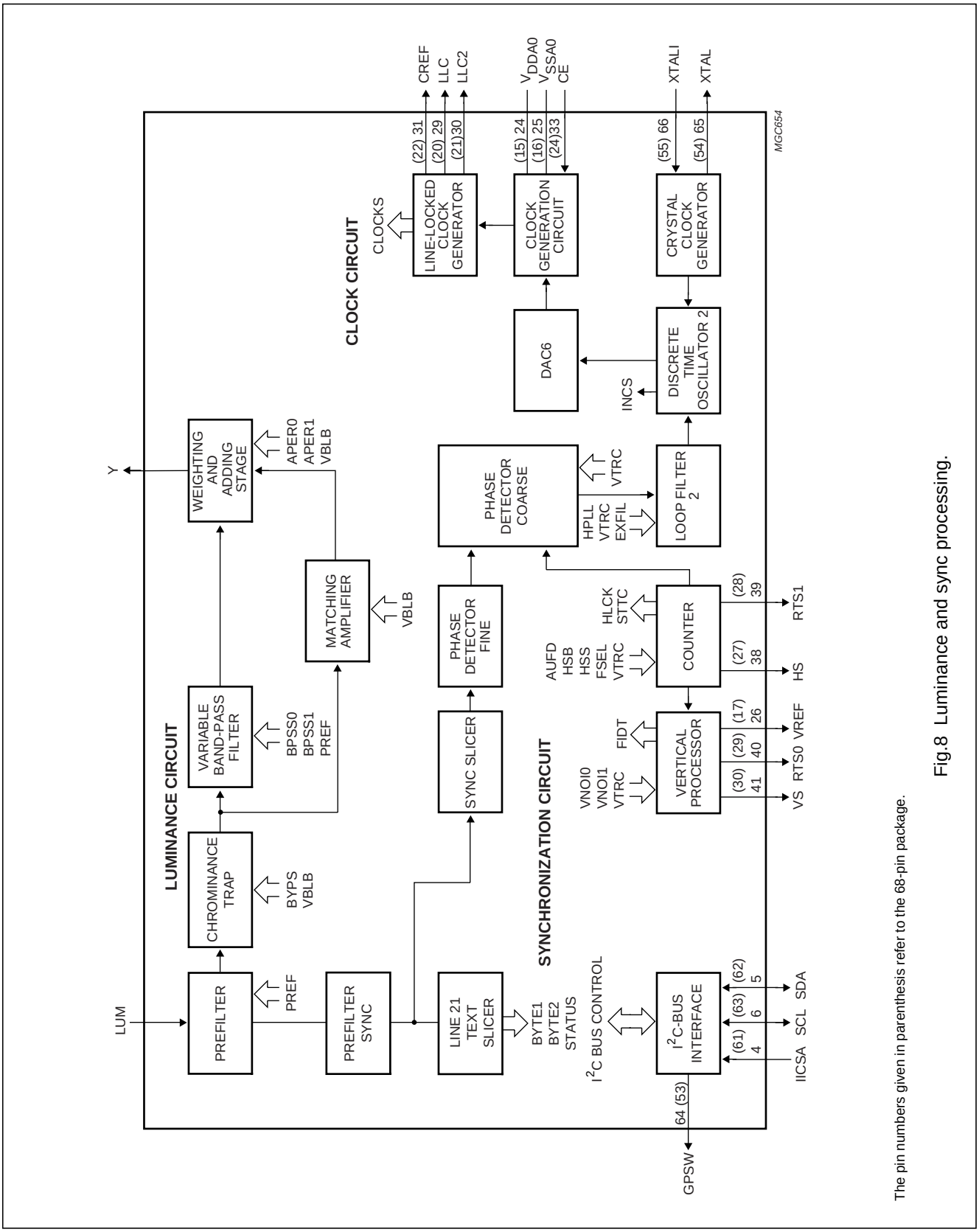
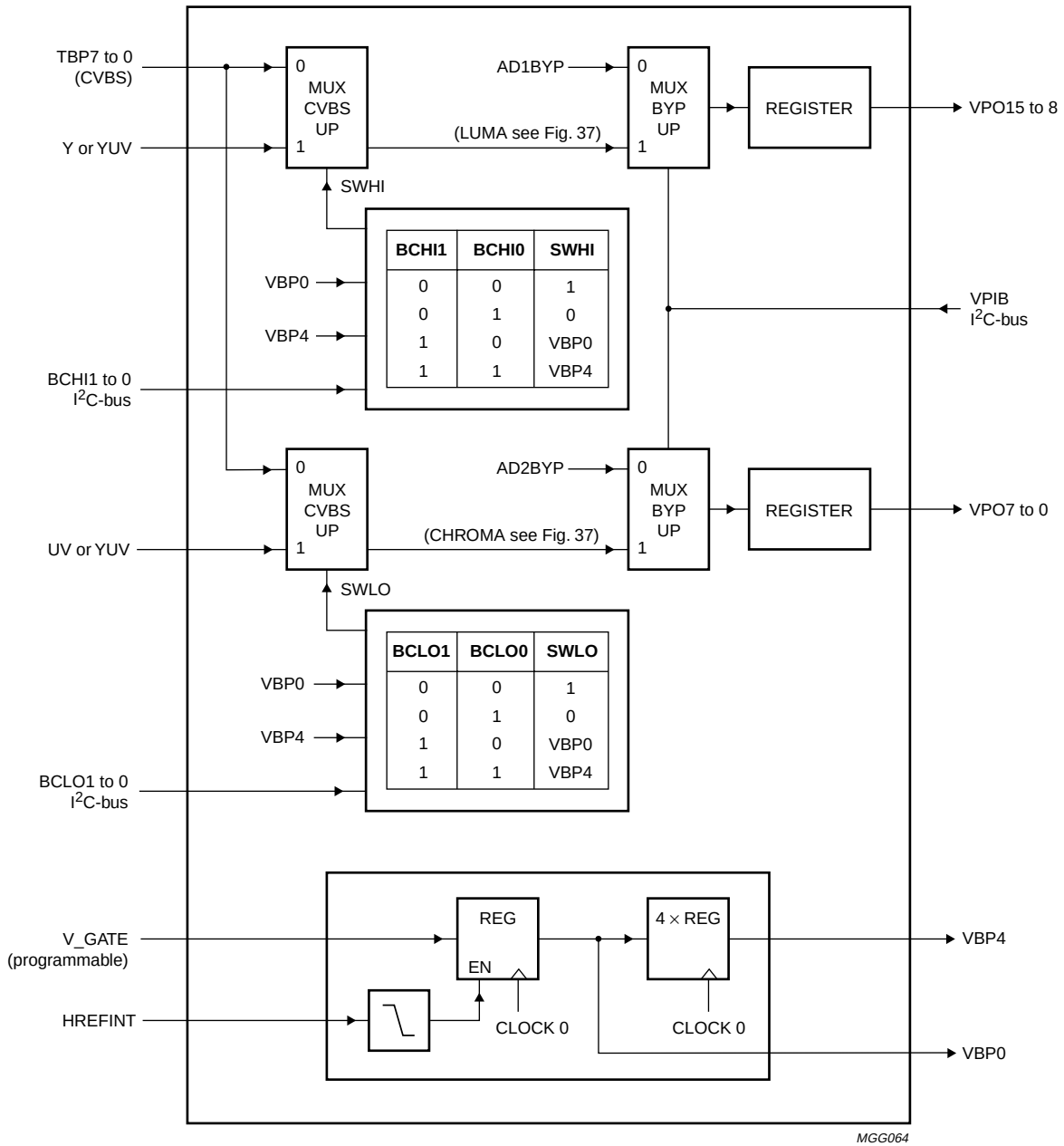


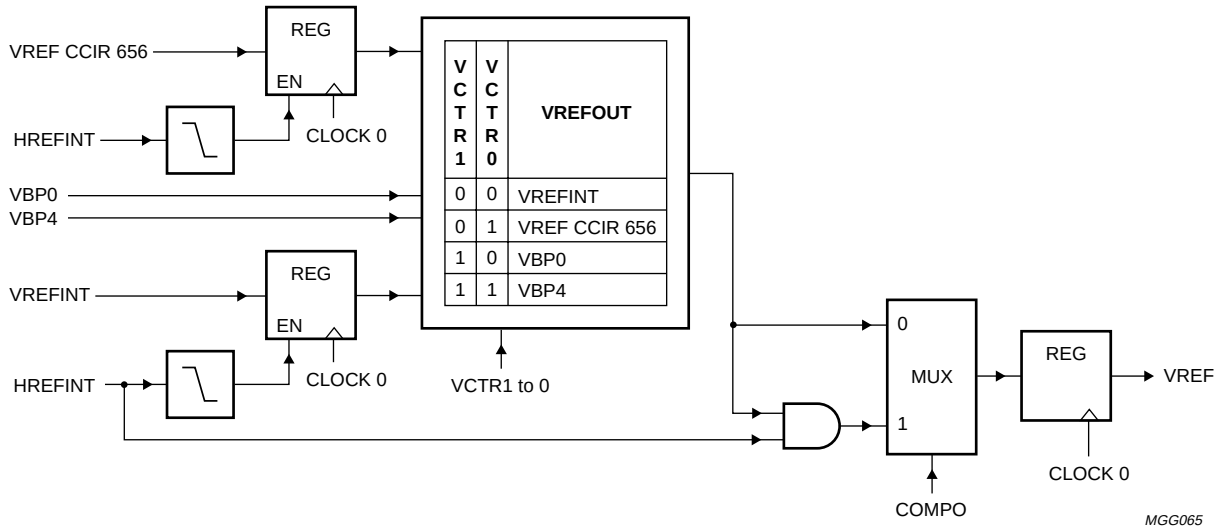
Fig.8 Luminance and sync processing.

The pin numbers given in parenthesis refer to the 68-pin package.



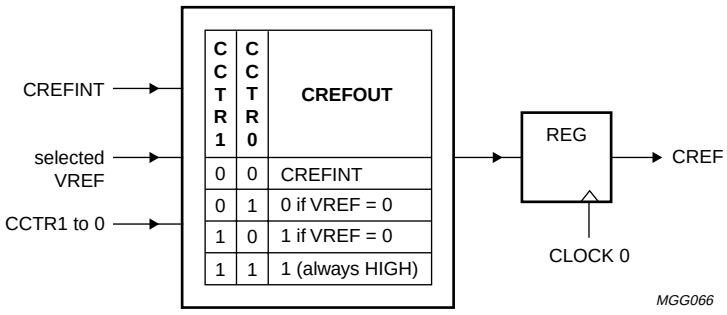
HREFINT = internal horizontal reference.
TBP = upsampled CVBS input data (27 MHz).
AD1BYP/AD2BYP = digitized CVBS input data and Y/C input data (13.5 MHz).
VBP0 = programmable vertical reference signal.
VBP4 = delayed programmable vertical reference signal (4LLC clocks delay).

Fig.9 Multiplexing of the CVBS signal to the VPO-bus.



VREF_CCIR 656 = vertical reference signal referring to the field interval definitions of CCIR656.
HREFINT = internal horizontal reference signal.
VREFINT = internal vertical reference signal.
VBP0 = programmable vertical reference signal.
VBP4 = delayed programmable vertical reference signal (4LLC clocks delay).

Fig.10 VREF output signal generation.



CREFINT = internal clock qualifier signal.

Fig.11 CREF output signal generation.

9 BOUNDARY-SCAN TEST

The SAA7111A has built in logic and 5 dedicated pins to support boundary-scan testing which allows board testing without special hardware (nails). The SAA7146 follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture*" set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRST), Test Data Input (TDI) and Test Data Output (TDO).

The BST functions BYPASS, EXTEST, INTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 1). Details about the JTAG BST-TEST can be found in the specification "*EEE Std. 1149.1"*. A file containing the detailed Boundary-Scan Description Language (BSDL) description of the SAA7111A is available on request.

9.1 Initialization of boundary-scan circuit

The TAP controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BTPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRST pin LOW.

9.2 Device identification codes

A Device Identification Register (DIR) is specified in *"IEEE Std. 1149.1-1990 - IEEE Standard Test Access Port and Boundary-Scan Architecture*" (IEEE Std. 1149.1b-1994). It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDI and TDO of the IC.
The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number.
The device identification register contains 32-bits, numbered 31 to 0, where bit 31 is the Most Significant Bit (MSB) (nearest to TDI) and bit 0 is the Least Significant Bit (LSB) (nearest to TDO); see Fig.12.

Table 1 BST instructions supported by the SAA7111A

INSTRUCTION	DESCRIPTION
BYPASS	this mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required
EXTEST	this mandatory instruction allows testing of off-chip circuitry and board level interconnections
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary-scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary-scan register is in external test mode.
IDCODE	this optional instruction will provide information on the components manufacturer, part number and version number
INTEST	this optional instruction allows testing of the internal logic (no support for customers available)
USER1	this private instruction allows testing by the manufacturer (no support for customers available)

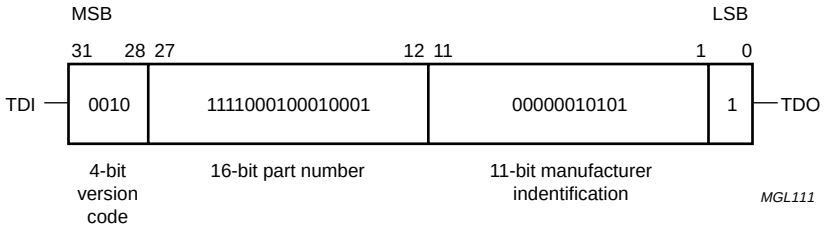


Fig.12 32 bits of identification code.

10 GAIN CHARTS

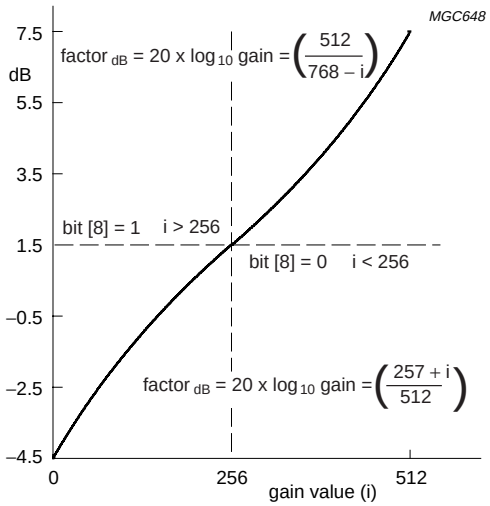
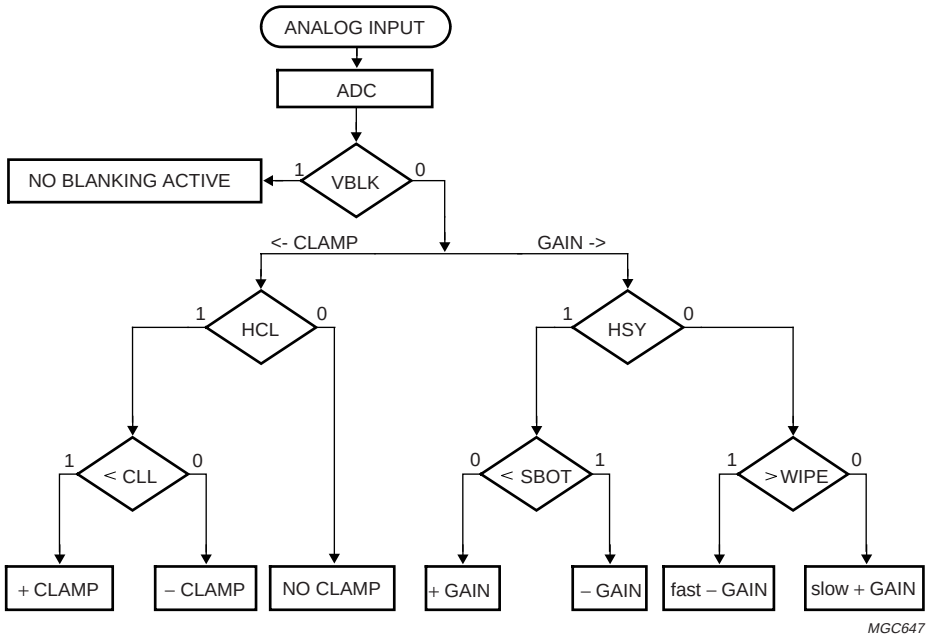
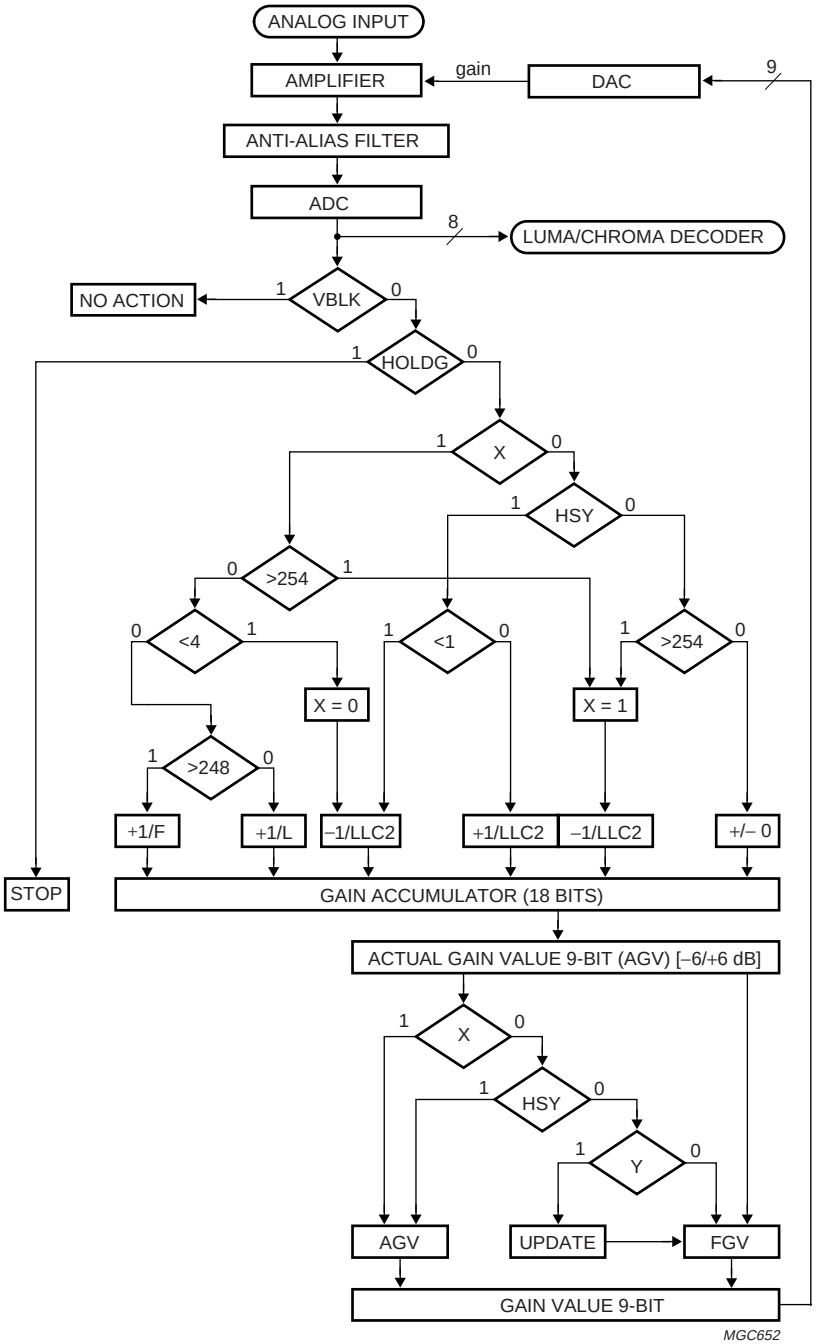


Fig.13 Amplifier curve.



WIPE = white peak level (254); SBOT = sync bottom level (1); CLL = clamp level [60 Y (128 C)];
HSY = horizontal sync pulse; HCL = horizontal clamp pulse.

Fig.14 Clamp and gain flow.



X = system variable; Y = IAGV – FGVI > GUDL; VBLK = vertical blanking pulse;
HSY = horizontal sync pulse; AGV = actual gain value; FGV = frozen gain value.

Fig.15 Gain flow chart.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all ground pins connected together and all supply pins connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.5	+4.6	V
V_{DDA}	analog supply voltage		–0.5	+4.6	V
V_i	input voltage		–0.5	V_{DD} + 0.5 (4.6 max)	V
V_o	output voltage		–0.5	V_{DD} + 0.5 (4.6 max)	V
ΔV_{SS}	voltage difference between V_{SSAall} and V_{SSall}		–	100	mV
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
$T_{amb(bias)}$	operating ambient temperature under bias		–10	+80	°C
V_{esd}	electrostatic discharge all pins	note 1	–2000	+2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

12 CHARACTERISTICS

V_{DDD} = 3.0 to 3.6 V; V_{DDA} = 3.1 to 3.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current		–	63	70	mA
P_D	digital power		–	0.21	–	W
V_{DDA}	analog supply voltage		3.1	3.3	3.5	V
I_{DDA}	analog supply current		–	63	–	mA
P_A	analog power		–	0.21	–	W
P_{A+D}	analog and digital power		–	0.42	–	W
Analog part						
I_{clamp}	clamping current	V_I = 0.9 V DC	–	±3.5	–	µA
$V_{i(p-p)}$	input voltage (peak-to-peak value)	for normal video levels [1 V (p-p)]; –3 dB termination 27/47 Ω and AC coupling required; coupling capacitor = 22 nF	0.3	0.7	1.2	V
$\|Z_i\|$	input impedance	clamping current off	200	–	–	kΩ
C_i	input capacitance		–	–	10	pF
α_{cs}	channel crosstalk	f_i = 5 MHz	–	–	–50	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converters						
B	bandwidth	at –3 dB	–	15	–	MHz
ϕ_{diff}	differential phase (amplifier plus anti-alias filter = bypass)		–	2	–	deg
G_{diff}	differential gain (amplifier plus anti-alias filter = bypass)		–	2	–	%
f_{clkADC}	ADC clock frequency		12.8	–	14.3	MHz
DLE	DC differential linearity error		–	0.7	–	LSB
ILE	DC integral linearity error		–	1	–	LSB
Digital inputs						
$V_{IL(SCL,SDA)}$	LOW level input voltage pins SDA and SCL		–0.5	–	$+0.3V_{DDD}$	V
V_{IH}	HIGH level input voltage pins SDA and SCL		$0.7V_{DDD}$	–	V_{DDD} + 0.5	V
$V_{IL(xtal)}$	LOW level CMOS input voltage pin XTALI		–0.3	–	+0.8	V
$V_{IH(xtal)}$	HIGH level CMOS input voltage pin XTALI		2.0	–	V_{DDD} + 0.3	V
V_{ILn}	LOW level input voltage all other inputs		–0.3	–	+0.8	V
V_{IHn}	HIGH level input voltage all other inputs		2.0	–	5.5	V
I_{LI}	input leakage current		–	–	1	µA
C_i	input capacitance	inputs and outputs at high-impedance	–	–	8	pF
$C_{i(n)}$	input capacitance all other inputs		–	–	5	pF
Digital outputs						
$V_{OL(SCL,SDA)}$	LOW level output voltage pins SDA and SCL	SDA/SCL at 3 mA (6 mA) sink current	–	–	0.4 (0.6)	V
V_{OL}	LOW level output voltage	V_{DDD} = min, I_{OL} = 2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	V_{DDD} = min, I_{OH} = –2 mA	2.4	–	V_{DDD} + 0.5	V
$V_{OL(clk)}$	LOW level output voltage for clocks		–0.5	–	+0.6	V
$V_{OH(clk)}$	HIGH level output voltage for clocks		2.4	–	V_{DDD} + 0.5	V
$\overline{\text{FEI}}$ input timing						
$t_{SU;DAT}$	input data set-up time		13	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data and control output timing; note 1						
C_L	output load capacitance		15	–	40	pF
$t_{OHD;DAT}$	output hold time	C_L = 15 pF	4	–	–	ns
t_{PD}	propagation delay	C_L = 25 pF	–	–	20	ns
t_{PDZ}	propagation delay to 3-state		–	–	20	ns
Clock output timing (LLC and LLC2); note 2						
$C_{L(LLC)}$	output load capacitance		15	–	40	pF
T_{cy}	cycle time	LLC	35	–	39	ns
		LLC2	70	–	78	ns
δ_{LLC}	duty factors for t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}	C_L = 25 pF	40	–	60	%
t_r	rise time LLC, LLC2		–	–	5	ns
t_f	fall time LLC, LLC2		–	–	5	ns
t_d	delay time LLC output to LLC2 output	at 1.5 V; LLC/LLC2 = 25 pF	–4	–	+8	ns
Data qualifier output timing (CREF)						
$t_{OHD;CREF}$	output hold time	C_L = 15 pF	4	–	–	ns
$t_{PD;CREF}$	propagation delay from positive edge of LLC	C_L = 25 pF	–	–	20	ns
Clock input timing (XTALI)						
δ_{XTALI}	duty factor for t_{XTALIH}/t_{XTALI}	nominal frequency	40	–	60	%
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz field	–	15625	–	Hz
		60 Hz field	–	15734	–	Hz
$\Delta f_H/f_{Hn}$	permissible static deviation		–	–	5.7	%
Subcarrier PLL						
f_{SCn}	nominal subcarrier frequency	PAL BGHI	–	4433619	–	Hz
		NTSC M; NTSC-Japan	–	3579545	–	Hz
		PAL M	–	3575612	–	Hz
		PAL N	–	3582056	–	Hz
Δf_{SC}	lock-in range		±400	–	–	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_n	nominal frequency	3rd harmonic; note 3	–	24.576	–	MHz
$\Delta f/f_n$	permissible nominal frequency deviation		–	–	±50	10^{-6}
$\Delta Tf/f_n$	permissible nominal frequency deviation with temperature		–	–	±20	10^{-6}
CRYSTAL SPECIFICATION (X1)						
$T_{amb(X1)}$	operating ambient temperature		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_s	series resonance resistor		–	40	80	Ω
C_1	motional capacitance		–	1.5 ±20%	–	fF
C_0	parallel capacitance		–	3.5 ±20%	–	pF

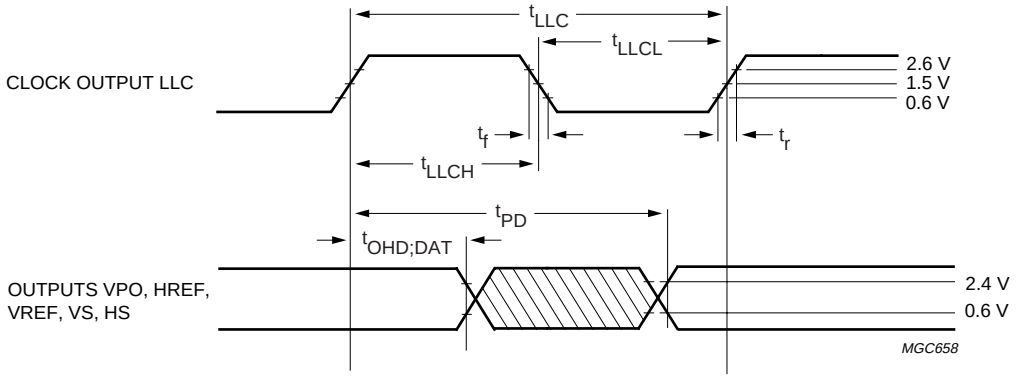
Notes

1. The levels must be measured with load circuits; 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.
2. The effects of rise and fall times are included in the calculation of $t_{OHD;DAT}$, t_{PD} and t_{PDZ}. Timings and levels refer to drawings and conditions illustrated in Figs 16 and 17.
3. Order number: Philips 4322 143 05291.

Table 2 Processing delay

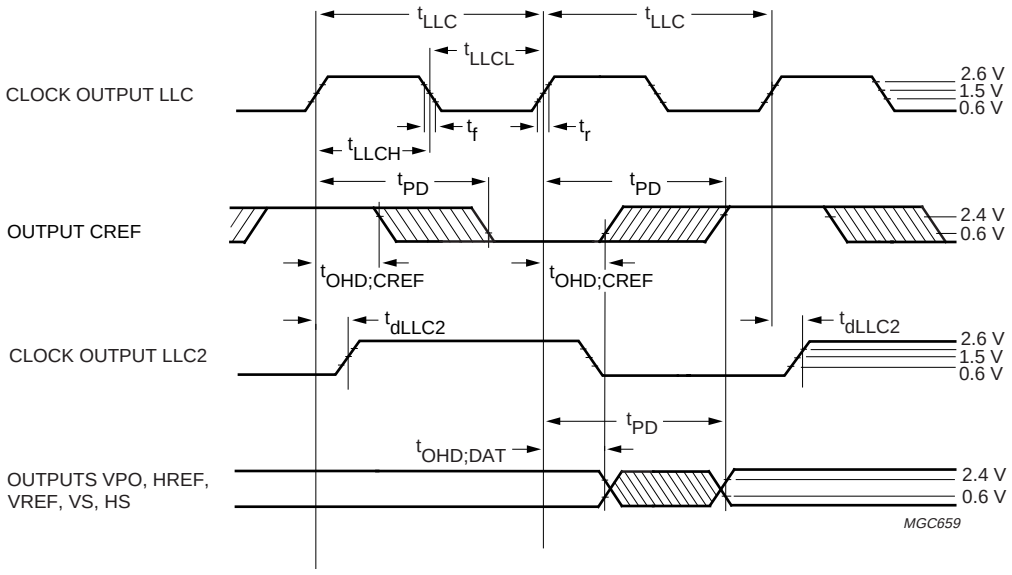
FUNCTION	TYPICAL ANALOG DELAY AI22 –> ADCIN (AOUT) (ns)	DIGITAL DELAY ADCIN –> VPO (LLC CLOCKS) [YDEL(2 to 0) = 000]
Without amplifier or anti-alias filter	15	179
With amplifier, without anti-alias filter	25	
With amplifier and anti-alias filter	75	

13 TIMING DIAGRAMS



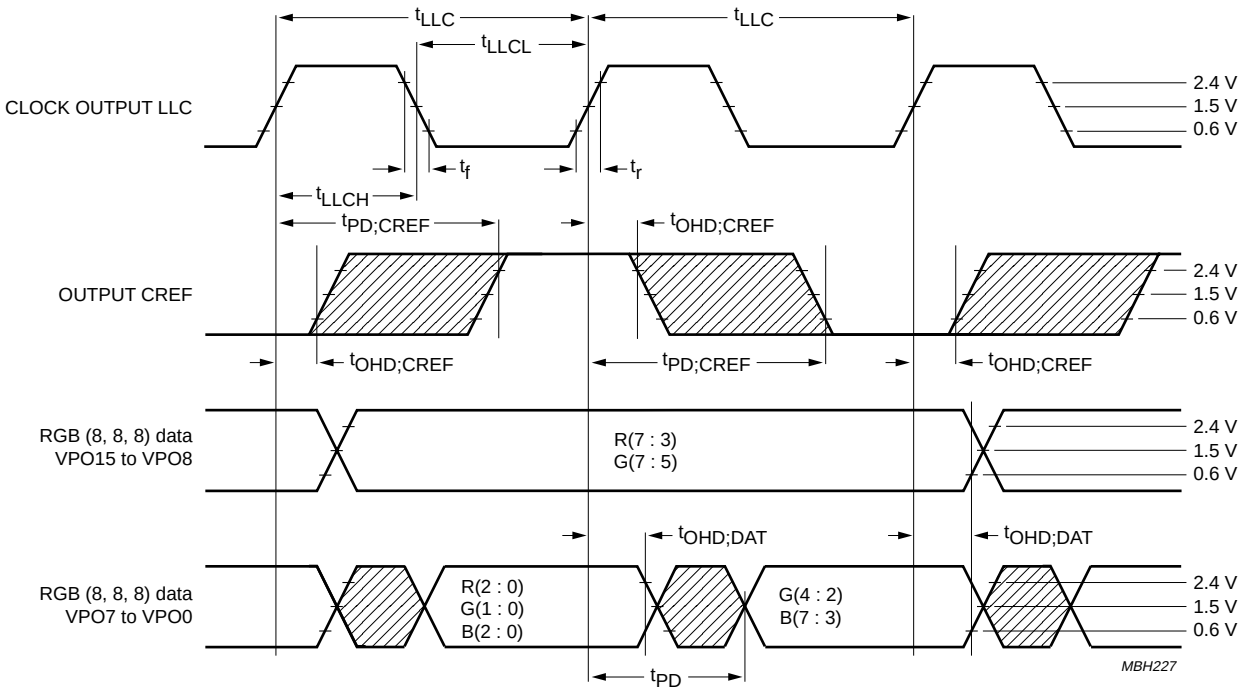
An explanation of the output formats is given in Table 6.

Fig.16 Clock/data timing (8-bit CCIR-656 format of the VPO-bus).



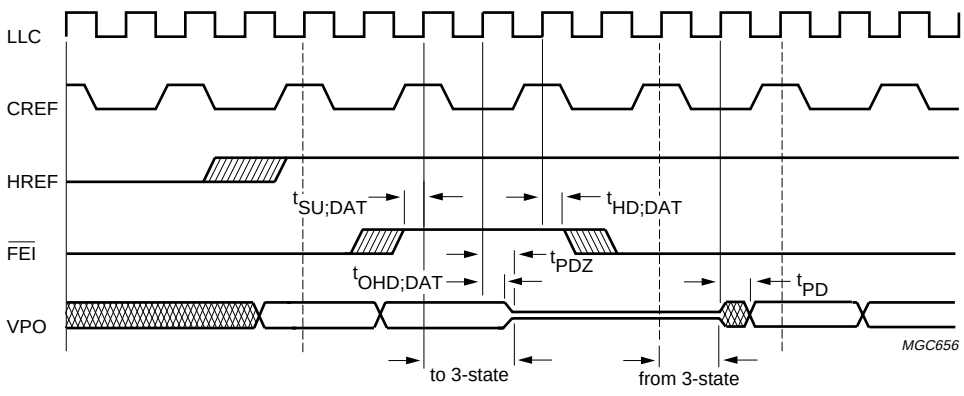
An explanation of the output formats is given in Table 6. The $\overline{FEI}$ timing of the VPO-bus is illustrated in Figs 19 and 20.

Fig.17 Clock/data timing (12 and 16-bit CCIR-601 format of the VPO-bus).



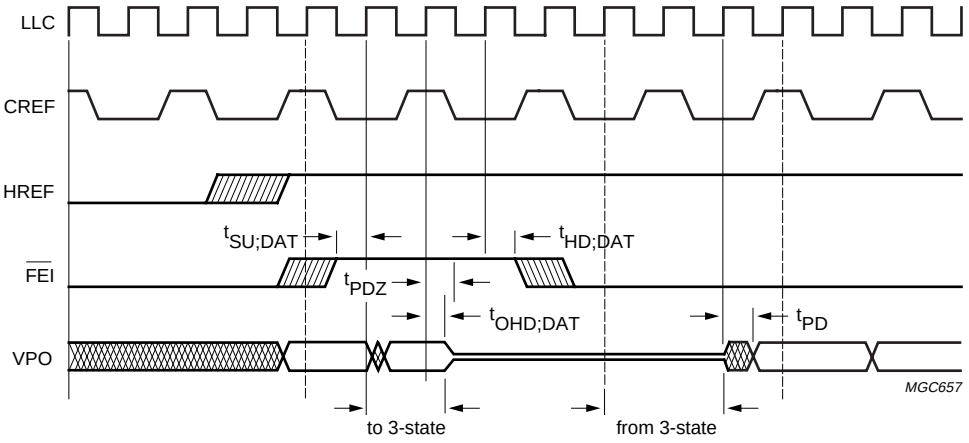
An explanation of the output formats is given in Table 6.

Fig.18 Clock/data timing for RGB (8, 8, 8) output format.



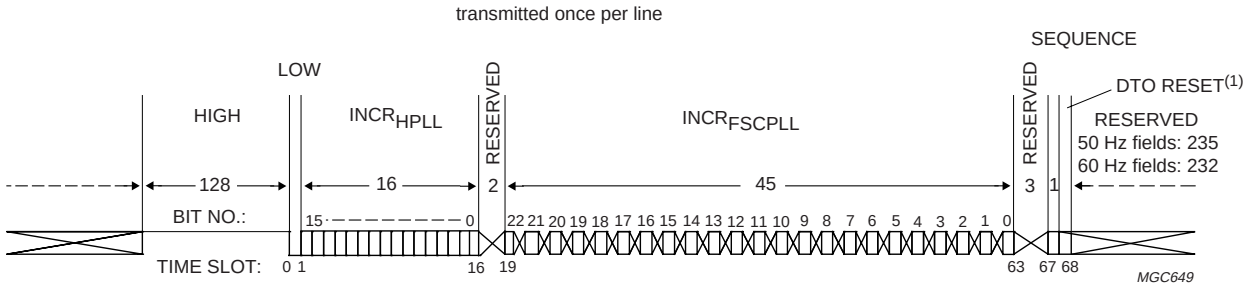
I^2C-bus bit FECO = 1.

Fig.19 $\overline{FEI}$ timing diagram ($\overline{FEI}$ sampling at CREF = HIGH) for OFTS = 0, 1 or 2).



Timing is compatible with SAA7110; I²C-bus bit FECO = 0.

Fig.20 $\overline{FEI}$ timing diagram ($\overline{FEI}$ sampling at CREF = LOW) for OFTS = 0, 1 or 2).



(1) Set to zero for one transmission, if a phase reset of the f_{sc} - DTO is applied via I²C-bus bit CDTO. RTCO sequence is generated in LLC/4.

The HPLL increment represents the actual LFCO frequency ($f_{LFCO} \times 4 = f_{LLC}$); 16 LSB from 20, upper four bits are fixed to 0100b

$$f_{LFCO} = \frac{INCR_{HPLL} \times f_{XTAL}}{2^{\text{word length DTO2}}}$$

Where: f_{XTAL} = 24.576 MHz, word length DTO2 = 20 bits.

The f_{sc} increment represents the actual subcarrier frequency (related to the actual clock); 23 LSB from 24, MSB is 0b.

$$f_{sc} = \frac{INCR_{FSCPLL} \times f_{XTAL}}{2^{\text{word length DTO1}}} \times \frac{INCR_{HPLL}}{2^{19}}$$

Where: word length DTO1 = 24 bits.

Fig.21 Real time control output.

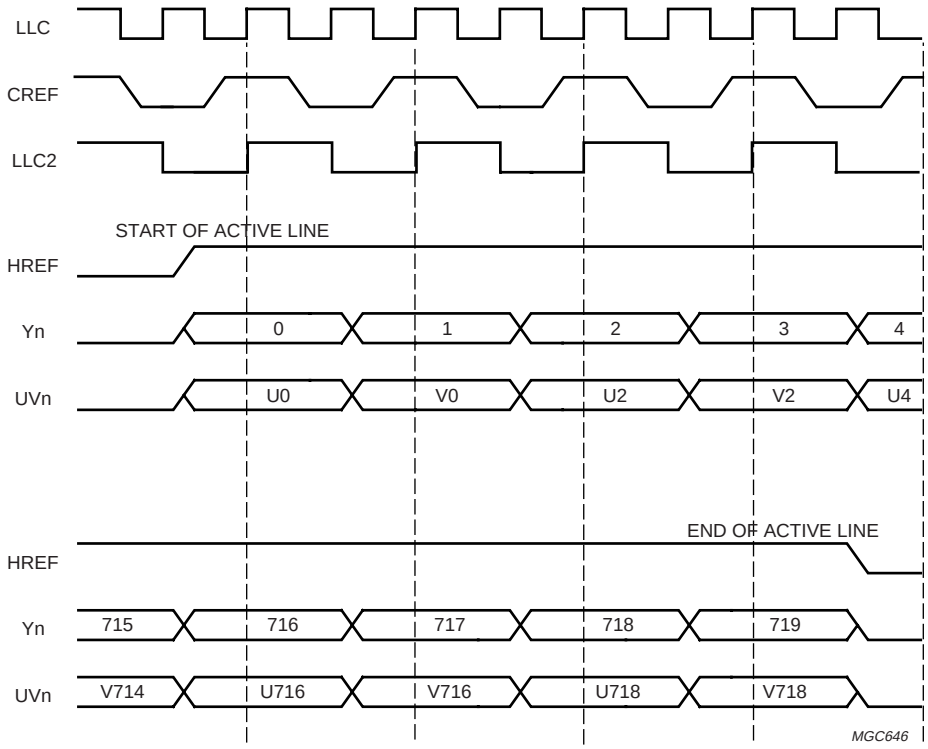


Fig.22 HREF timing diagram.

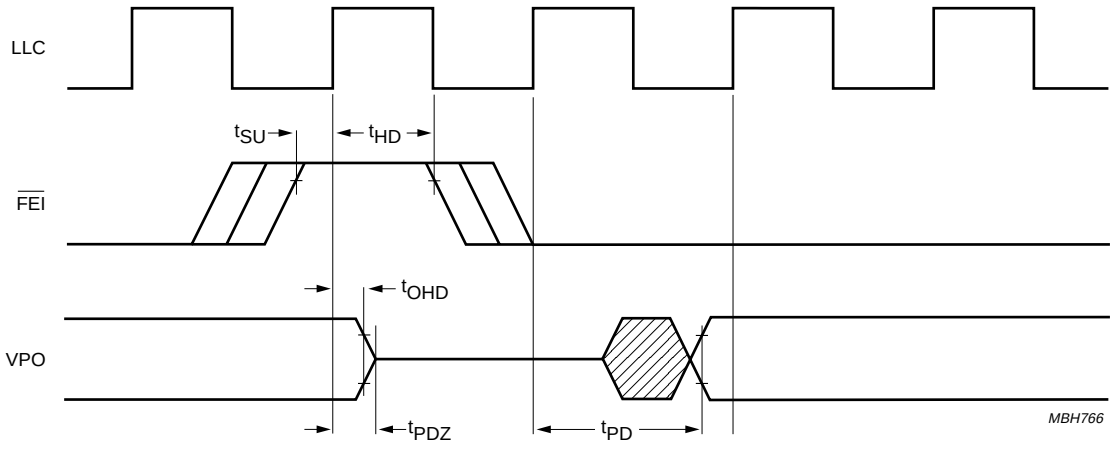
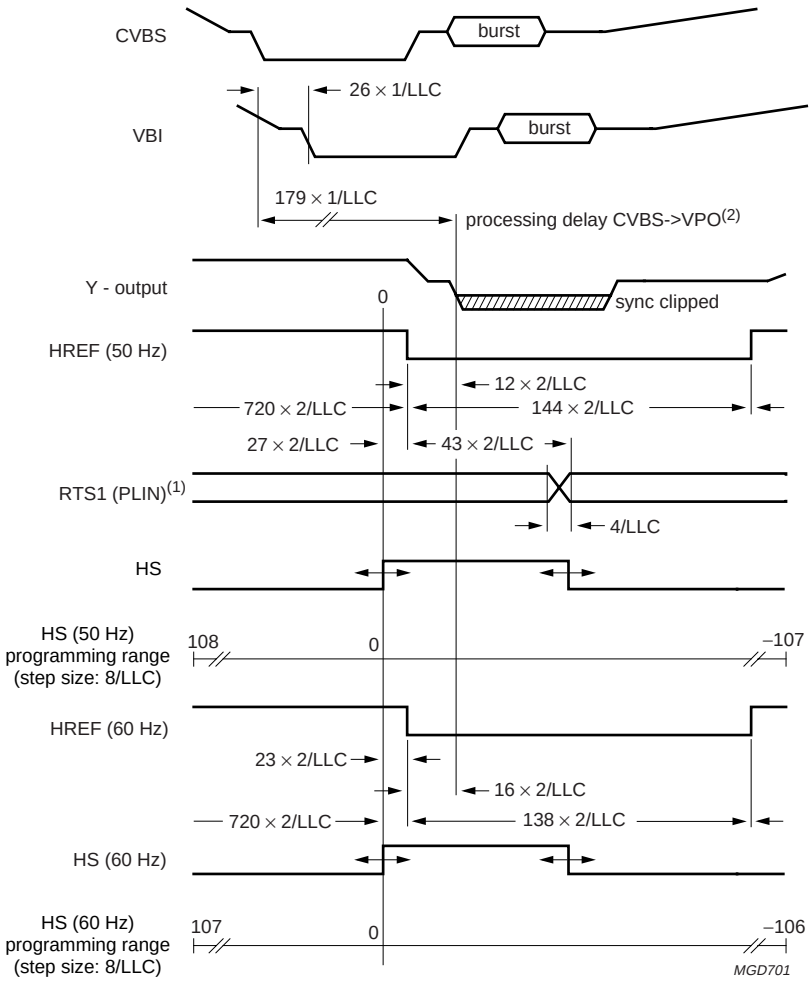


Fig.23 $\overline{\text{FEI}}$ timing in CCIR 656 mode [OFTS (1 : 0) = 3].

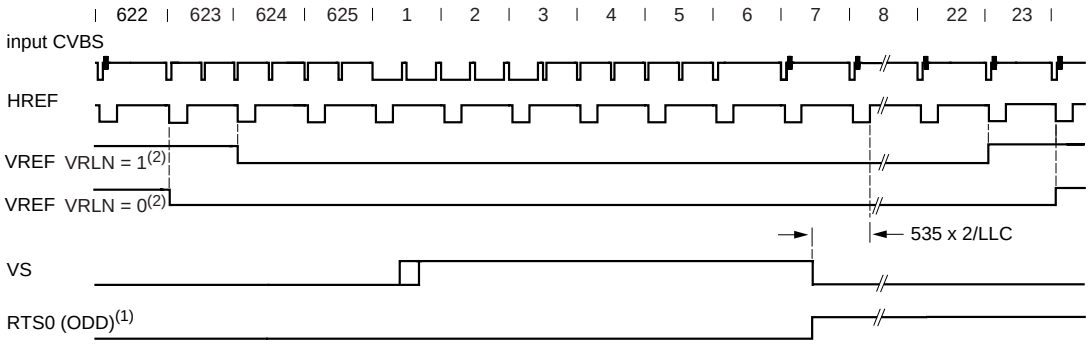


(1) PLIN is switched to output RTS1 via I²C-bus bit RTSE1 = 0.

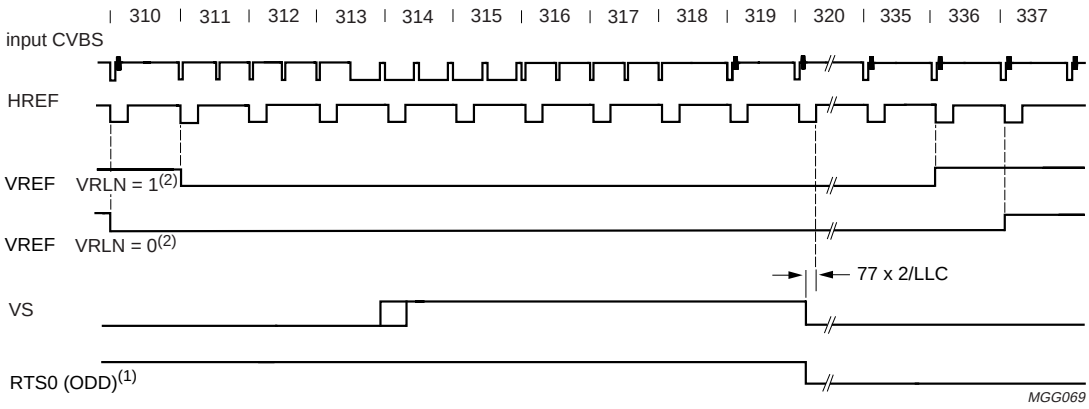
(2) See Table 2.

(3) HDEL (1 : 0) = 0 0, YDEL (2 : 0) = 0 0 0.

Fig.24 Horizontal timing diagram.



(a) 1st field



(b) 2nd field

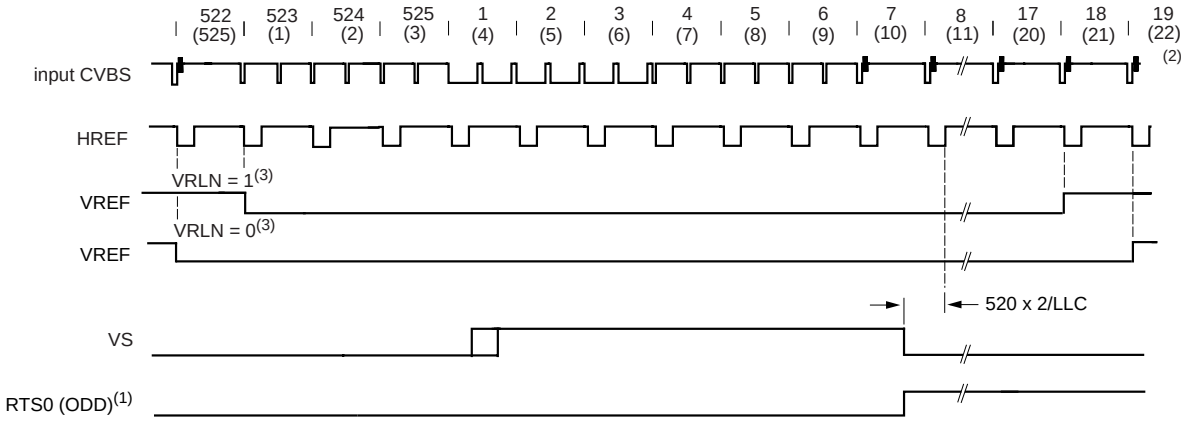
(1) ODD is switched to output RTS0 via I²C-bus bit RTSE0 = 0.

(2) Additional VREF positions can be achieved via I²C-bits VCTR1 and VCTR0 (see Fig.10).

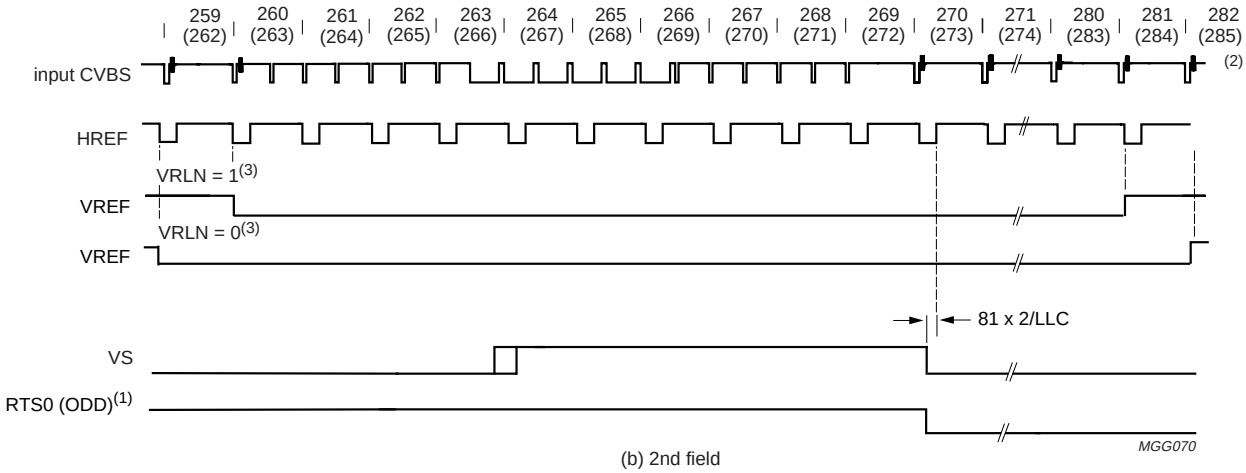
The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bus bit VBLB is set to logic 1.

The chrominance delay line (chrominance-comb filter for NTSC, phase error correcting for PAL) is disabled during VREF = 0.

Fig.25 Vertical timing diagram for 50 Hz [nominal input signal VNL in normal mode (VNOI = 00b)].



(a) 1st field



(b) 2nd field

(1) ODD is switched to output RTS0 via I²C-bus bit RTSE0 = 0.

(2) Line numbers in parenthesis refer to CCIR line counting.

(3) Additional VREF positions can be achieved via I²C-bus bits VCTR1 and VCTR0 (see Fig.10).

The luminance peaking and the chrominance trap are bypassed during VREF = 0 if I²C-bus bit VBLB is set to logic 1.

The chrominance delay line (chrominance-comb filter for NTSC, phase error correcting for PAL) is disabled during VREF = 0.

Fig.26 Vertical timing diagram for 60 Hz [nominal input signal VNL in normal mode (VNOI = 00b)].

Table 3 Digital output control

OEYC	$\overline{FEI}$	VPO
		15 to 0
0	0	Z
1	0	active
0	1	Z
1	1	Z

Table 4 Clock frequencies

CLOCK	FREQUENCY (MHz)
XTAL	24.576
LLC	27
LLC2	13.5
LLC4	6.75
LLC8	3.375

14 CLOCK SYSTEM

14.1 Clock generation circuit

The internal CGC generates the system clocks LLC, LLC2 and the clock reference signal CREF. The internally generated LFCO (triangular waveform) is multiplied by 2 or 4 via the analog PLL (including phase detector, loop filter, VCO and frequency divider). The rectangular output signals have a 50% duty factor.

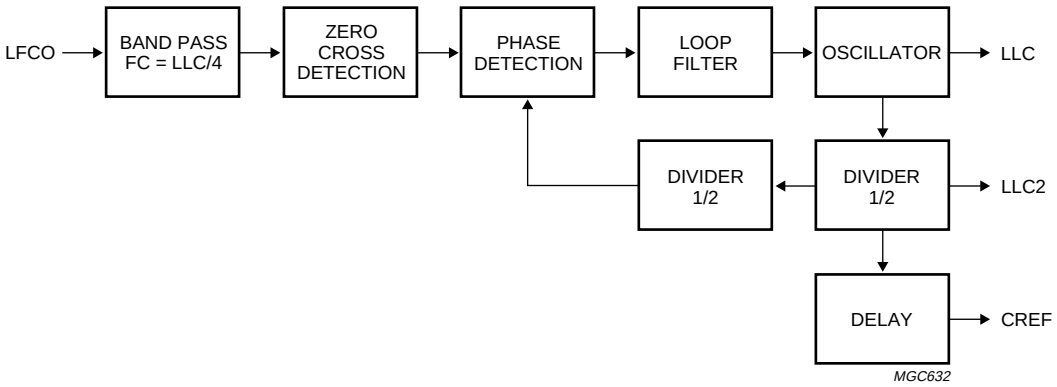
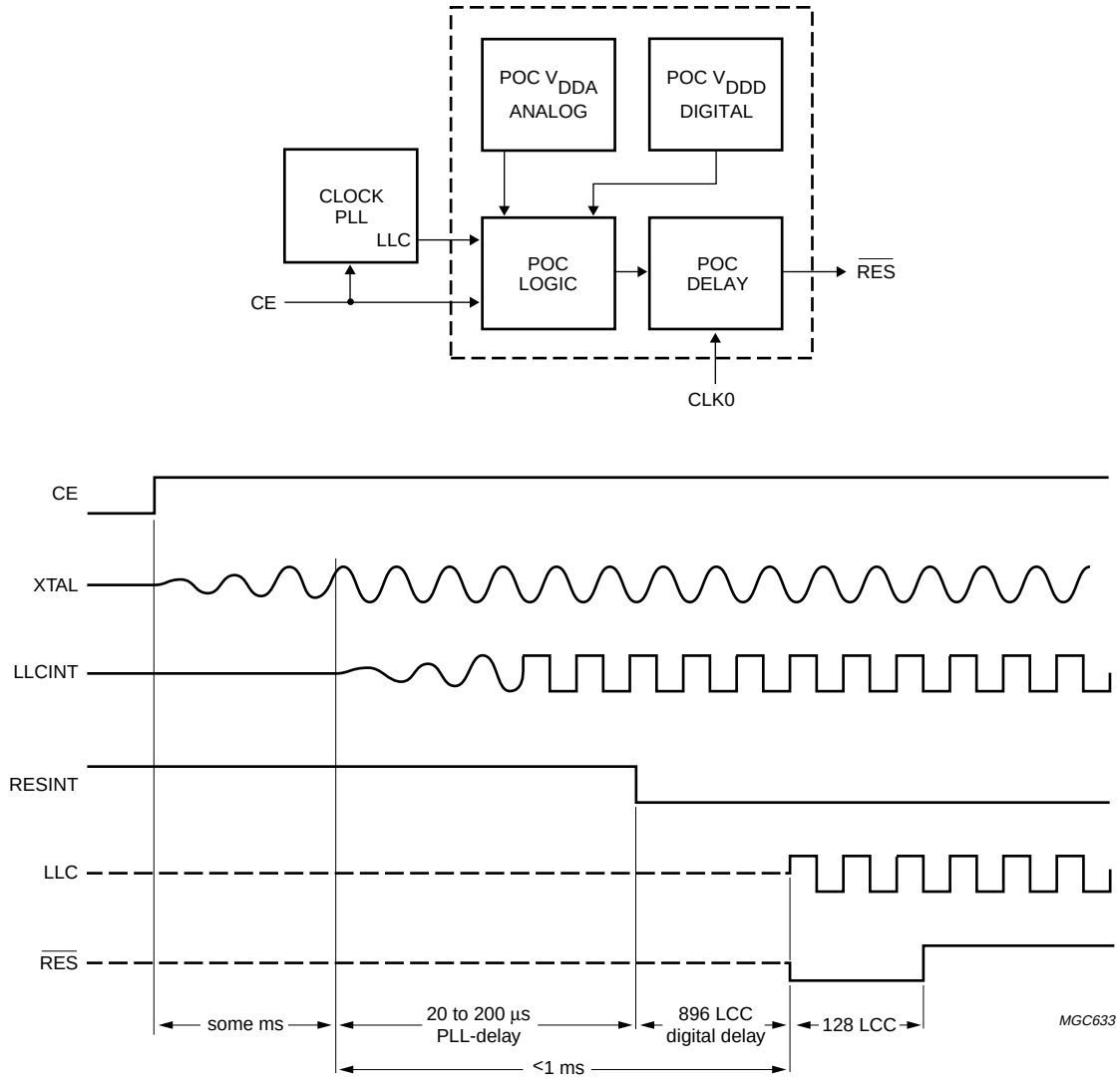


Fig.27 Block diagram of clock generation circuit.

14.2 Power-on control

Power-on reset is activated at power-on, chip enable, PLL clock generation failure and if the supply voltage falls below 2.7 V. The $\overline{RES}$ signal can be applied to reset other circuits of the digital picture processing system.



CE = chip enable input; XTAL = crystal oscillator output; LLCINT = internal system clock; RESINT = internal reset; LLC = line-locked clock output; $\overline{RES}$ = reset output (active LOW).

Fig.28 Power-on control circuit.

Table 5 Power-on control sequence

INTERNAL POWER-ON CONTROL SEQUENCE	PIN OUTPUT STATUS	FUNCTION
Directly after power-on asynchronous reset	VPO15 to VPO0, RTCO, RTS0, RTS1, GPSW, HREF, VREF, HS, VS, LLC, LLC2 and CREF are in high-impedance state	direct switching to high impedance for 20 to 200 ms
Synchronous reset sequence	LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA become active; VPO15 to VPO0, HREF, VREF, HS and VS are held in high-impedance state	internal reset sequence
Status after power-on control sequence	VPO15 to VPO0, HREF, VREF, HS and VS are held in high-impedance state	after power-on (reset sequence) a complete I^2C-bus transmission is required

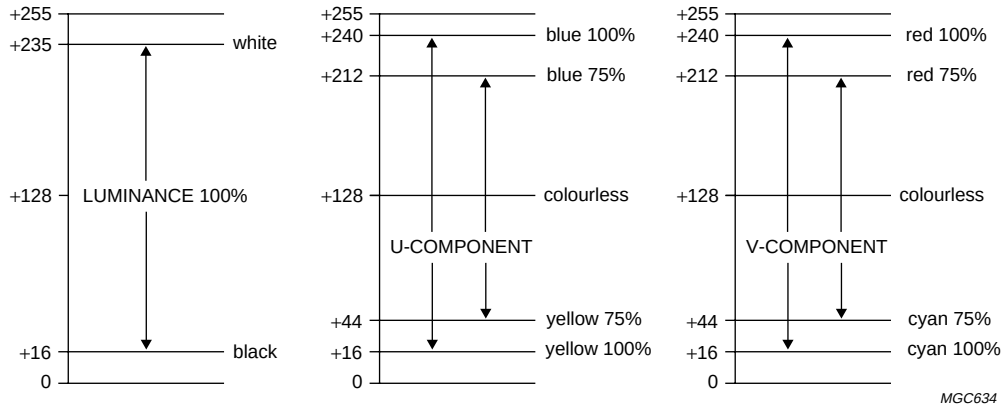
15 OUTPUT FORMATS

Table 6 Output formats of the VPO bus (note 1)

BUS SIGNAL	411 (12-BIT)				422 (16-BIT)(2)		CCIR-656 (8-BIT)(3)				RGB (16-BIT)(4)	RGB (24-BIT)(4)	
VPO15	Y_{07}	Y_{17}	Y_{27}	Y_{37}	Y_{07}	Y_{17}	U_{07}	Y_{07}	V_{07}	Y_{17}	R4	R7	R7
VPO14	Y_{06}	Y_{16}	Y_{26}	Y_{36}	Y_{06}	Y_{16}	U_{06}	Y_{06}	V_{06}	Y_{16}	R3	R6	R6
VPO13	Y_{05}	Y_{15}	Y_{25}	Y_{35}	Y_{05}	Y_{15}	U_{05}	Y_{05}	V_{05}	Y_{15}	R2	R5	R5
VPO12	Y_{04}	Y_{14}	Y_{24}	Y_{34}	Y_{04}	Y_{14}	U_{04}	Y_{04}	V_{04}	Y_{14}	R1	R4	R4
VPO11	Y_{03}	Y_{13}	Y_{23}	Y_{33}	Y_{03}	Y_{13}	U_{03}	Y_{03}	V_{03}	Y_{13}	R0	R3	R3
VPO10	Y_{02}	Y_{12}	Y_{22}	Y_{32}	Y_{02}	Y_{12}	U_{02}	Y_{02}	V_{02}	Y_{12}	G5	G7	G7
VPO9	Y_{01}	Y_{11}	Y_{21}	Y_{31}	Y_{01}	Y_{11}	U_{01}	Y_{01}	V_{01}	Y_{11}	G4	G6	G6
VPO8	Y_{00}	Y_{10}	Y_{20}	Y_{30}	Y_{00}	Y_{10}	U_{00}	Y_{00}	V_{00}	Y_{10}	G3	G5	G5
VPO7	U_{07}	U_{05}	U_{03}	U_{01}	U_{07}	V_{07}	X	X	X	X	G2	G4	R2
VPO6	U_{06}	U_{04}	U_{02}	U_{00}	U_{06}	V_{06}	X	X	X	X	G1	G3	R1
VPO5	V_{07}	V_{05}	V_{03}	V_{01}	U_{05}	V_{05}	X	X	X	X	G0	G2	R0
VPO4	V_{06}	V_{04}	V_{02}	V_{00}	U_{04}	V_{04}	X	X	X	X	B4	B7	G1
VPO3	X	X	X	X	U_{03}	V_{03}	X	X	X	X	B3	B6	G0
VPO2	X	X	X	X	U_{02}	V_{02}	X	X	X	X	B2	B5	B2
VPO1	X	X	X	X	U_{01}	V_{01}	X	X	X	X	B1	B4	B1
VPO0	X	X	X	X	U_{00}	V_{00}	X	X	X	X	B0	B3	B0
Pixel order Y	0	1	2	3	0	1	0		1		–	note 6	note 5
Pixel order UV	0				0		0				–	–	
Data rates	LLC2				LLC2		LLC				LLC2	–	
I^2C-bus control signals	OFTS0 = 0				OFTS0 = 1		OFTS0 = 1				OFTS0 = 0	OFTS0 = 0	
	OFTS1 = 1				OFTS1 = 0		OFTS1 = 1				OFTS1 = 0	OFTS1 = 0	
	RGB888 = X				RGB888 = X		RGB888 = X				RGB888 = 0	RGB888 = 1	

Notes to Table 5

1. VPO bus allows connection to 5 V video data bus systems.
2. Values in accordance with CCIR 601.
3. Before and after the video data, video timing codes are inserted in accordance with CCIR 656.
   a) VPO15 to VPO8 = VPO7 to VPO0 = CCIR 656 data if I²C-bus bit TCLO = 0
   b) VPO15 to VPO8 = CCIR 656 data, VPO7 to VPO0 = 3-state if I²C-bus bit TCLO = 1.
4. During HREF = LOW RGB levels are set to 16 (10 hex). RGB 16-bit is achieved by dropping the LSBs of the 8-bit signals (after dithering if desired).
5. CREF = 1 (see Fig.18).
6. CREF = 0 (see Fig.18).



(a) Y output range. (b) U output range (Cb). (c) V output range (Cr).

CCIR Rec. 602 digital levels.

Equations for modification to the YUV levels via BCS control I²C-bus bytes BRIG, CONT and SATN.

Luminance:

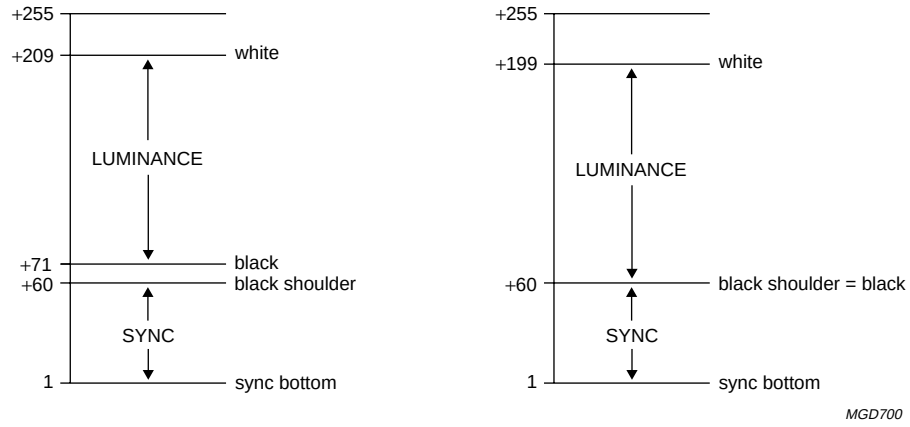
$$Y_{OUT} = Int\left[\frac{CONT}{71} \times (Y - 128)\right] + BRIG$$

Chrominance:

$$UV_{OUT} = Int\left[\frac{SATN}{64} \times (Cr, Cb - 128)\right] + 128$$

It should be noted that the resulting levels are limited to 1 to 254 in accordance with CCIR-601/656 standard.

Fig.29 VPO output signal range with default BCS settings.

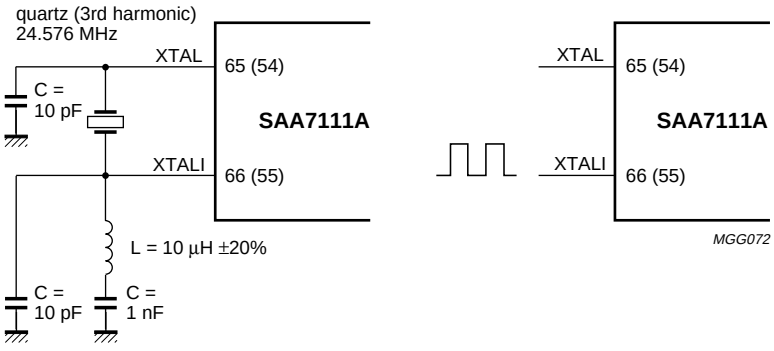


(a) For sources containing 7.5 IRE black level offset (e.g. NTSC–M).

(b) For sources not containing black level offset.

VBI data levels are **not** dependent on BCS settings.

Fig.30 VBI data bypass output range.



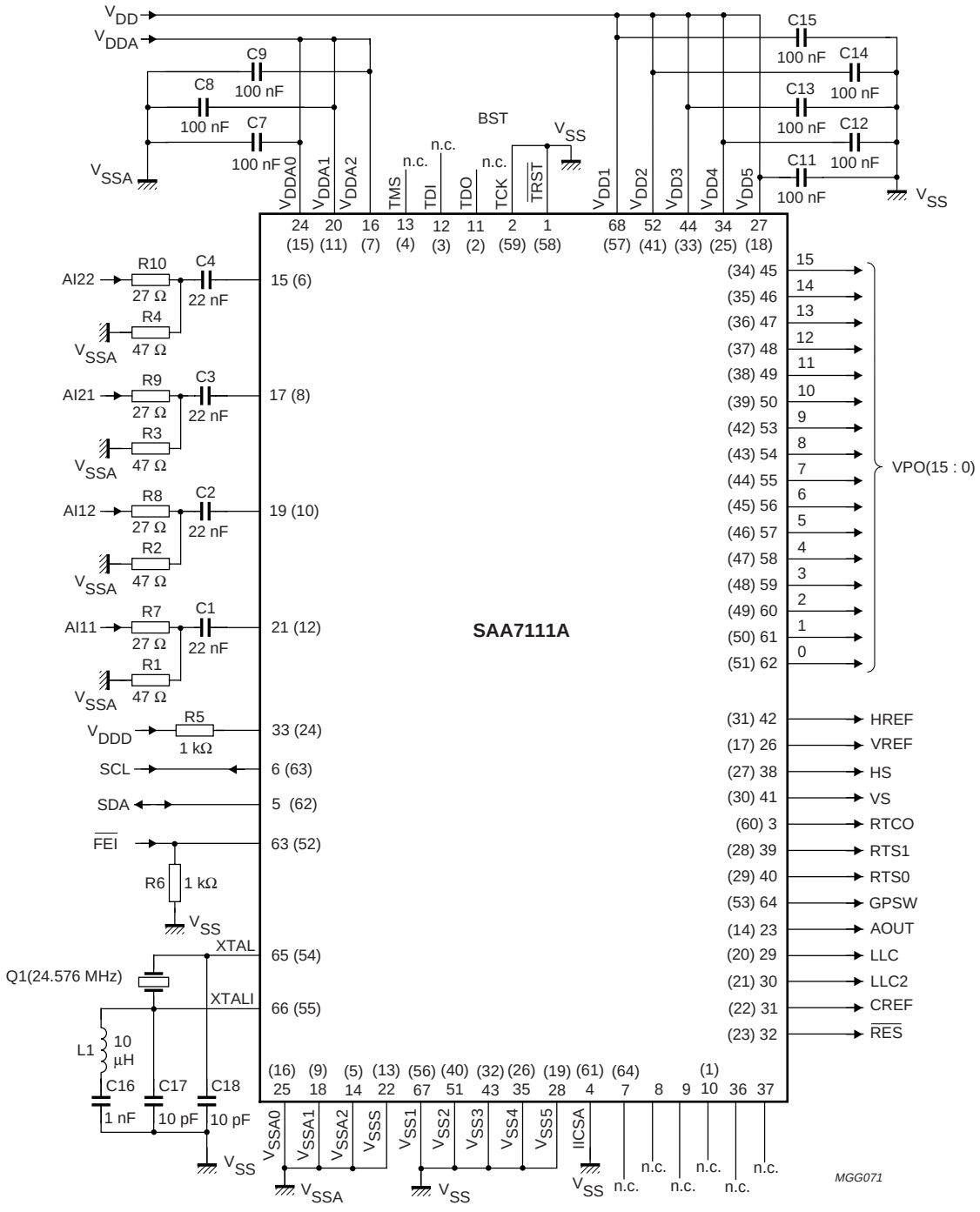
(a) With quartz crystal.

(b) With external clock.

The pin numbers given in parenthesis refer to the 64-pin package.
Order number: Philips 4322 143 05291.

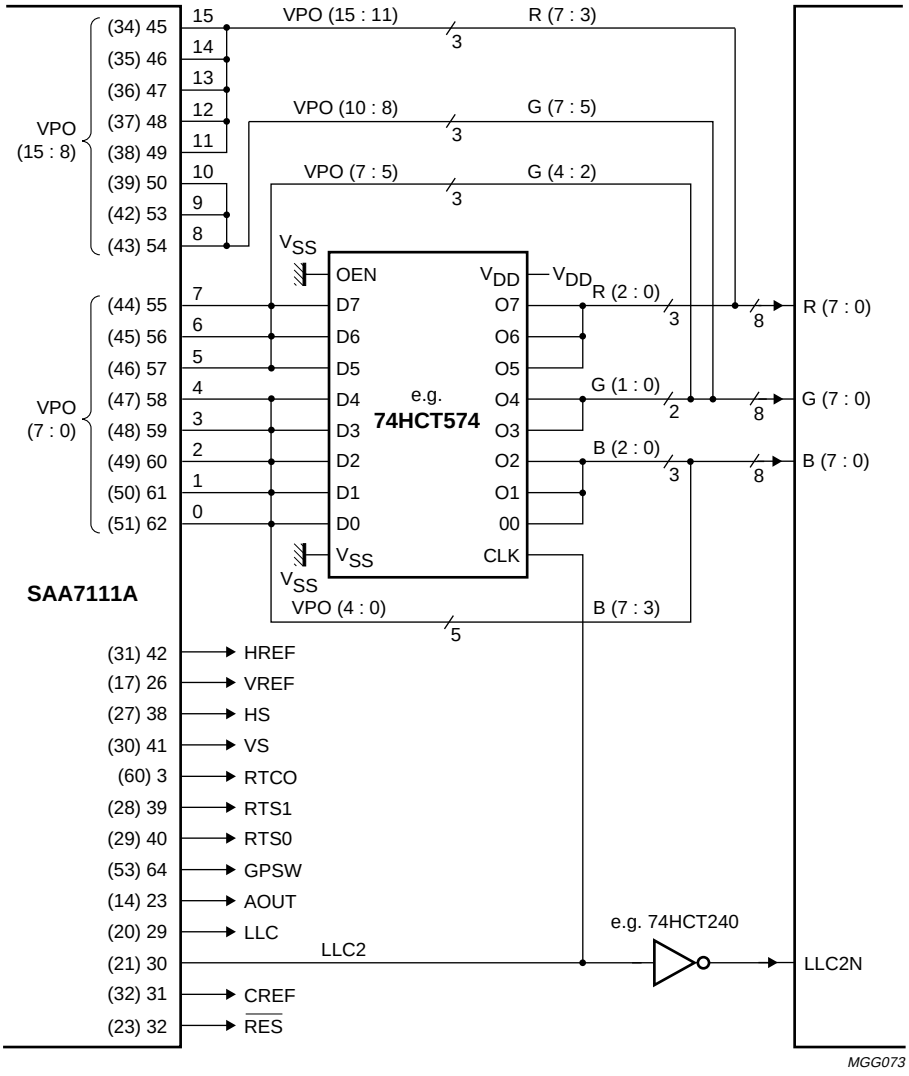
Fig.31 Oscillator application.

16 APPLICATION INFORMATION



The pin numbers given in parenthesis refer to the 64-pin package.

Fig.32 Application diagram.



The pin numbers given in parenthesis refer to the QFP64 package.

I²C-bus control bits:

OFTS(1 : 0) = 00 (subaddress 10H, bits D7 and D6).

RGB888 = 1 (subaddress 12H, bit D3).

Fig.33 Application diagram for RGB 24-bit output format.

17 I²C-BUS DESCRIPTION

17.1 I²C-bus format

Table 7 Write procedure

S	SLAVE ADDRESS W	ACK s	SUBADDRESS	ACK s	DATA (N BYTES)	ACK s	P

Table 8 Read procedure (combined format)

S	SLAVE ADDRESS W	ACK s	SUBADDRESS	ACK s	
Sr	SLAVE ADDRESS R	ACK s	DATA (N BYTES)	ACK m	P

Table 9 Description of I²C-bus format

CODE	DESCRIPTION	
S	START condition	
Sr	repeated START condition	
Slave address W	0100 1000b (IICSA = LOW) or 0100 1010b (IICSA = HIGH)	
Slave address R	0100 1001b (IICSA = LOW) or 0100 1011b (IICSA = HIGH)	
ACK s	acknowledge generated by the slave	
ACK m	acknowledge generated by the master	
Subaddress	subaddress byte, see Table 10	
Data	data byte, see Table 10; note 1	
P	STOP condition	
X = LSB slave address	read/write control bit; X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter)	
Slave address	read = 49h or 4Bh; note 2	
	write = 48h or 4Ah	
	IICSA = 0 or 1	
Subaddresses	00h chip version	read and write; note 3
	01h reserved	–
	02h to 05h front-end part	read and write
	06h to 13h decoder part	read and write
	14h reserved	–
	15h to 17h decoder part	read and write
	18h to 19h reserved	–
	1Ah to 1Ch Line-21 text slicer part	read only
	1Dh to 1Eh reserved	–
	1Fh status byte	read only

Notes

1. If more than one byte DATA is transmitted then the auto-increment of the subaddress is performed.
2. During slave transmitter mode the SCL-LOW period may be extended by pulling SCL to LOW (in accordance with the I²C-bus specification).
3. The I²C-bus subaddress 00 has to be initialized with 0 before being read.

Table 10 I²C-bus receiver/transmitter overview

SLAVE ADDRESS		READ		WRITE		IICSA			
		49H 4BH		48H 4AH		0 1			
REGISTER FUNCTION	**SUB-ADDR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Chip version	00	ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
Reserved	01	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Analog input contr 1	02	FUSE1	FUSE0	GUDL2	GUDL1	GUDL0	MODE2	MODE1	MODE0
Analog input contr 2	03	(1)	HLNRS	VBSL	WPOFF	HOLDG	GAFIX	GAI28	GAI18
Analog input contr 3	04	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
Analog input contr 4	05	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
Horizontal sync start	06	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
Horizontal sync stop	07	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
Sync control	08	AUFD	FSEL	EXFIL	(1)	VTRC	HPLL	VNOI1	VNOI0
Luminance control	09	BYPS	PREF	BPSS1	BPSS0	VBLB	UPTCV	APER1	APER0
Luminance brightness	0A	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
Luminance contrast	0B	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
Chroma saturation	0C	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
Chroma Hue control	0D	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
Chroma control	0E	CDTO	CSTD2	CSTD1	CSTD0	DCCF	FCTC	CHBW1	CHBW0
Reserved	0F	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Format/delay control	10	OFTS1	OFTS0	HDEL1	HDEL0	VRLN	YDEL2	YDEL1	YDEL0
Output control 1	11	GPSW	CM99	FECO	COMPO	OEYC	OEHV	VIPB	COLO
Output control 2	12	RTSE1	RTSE0	TCLO	CBR	RGB888	DIT	AOSL1	AOSL0
Output control 3	13	VCTR1	VCTR0	CCTR1	CCTR0	BCHI1	BCHI0	BCLO1	BCLO0
Reserved	14	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
V_GATE1_START	15	VSTA7	VSTA6	VSTA5	VSTA4	VSTA3	VSTA2	VSTA1	VSTA0
V_GATE1_STOP	16	VSTO7	VSTO6	VSTO5	VSTO4	VSTO3	VSTO2	VSTO1	VSTO0
V_GATE1_MSB	17	(1)	(1)	(1)	(1)	(1)	(1)	VSTO8	VSTA8
Reserved	18-19	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Text slicer status	1A	(1)	(1)	(1)	(1)	F2VAL	F2RDY	F1VAL	F1RDY
Decoded bytes of the text slicer	1B	P1	BYTE16	BYTE15	BYTE14	BYTE13	BYTE12	BYTE11	BYTE10
	1C	P2	BYTE26	BYTE25	BYTE24	BYTE23	BYTE22	BYTE21	BYTE20
Reserved	1D-1E	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Status byte	1F	STTC	HLCK	FIDT	GLIMT	GLIMB	WIPA	SLTCA	CODE

Note

1. All unused control bits must be programmed with logic 0.

17.2 I²C-bus detail

The I²C-bus receiver slave address is 48H/49H. Subaddresses 0F, 14, 18, 19, 1D and 1E are reserved; subaddress 01 is reserved for chip version.

17.2.1 SUBADDRESS 00

Table 11 Chip version SA00

FUNCTION		LOGIC LEVELS							
		ID07	ID06	ID05	ID04	ID03	ID02	ID01	ID00
Chip version	V1	0	0	0	1	X	X	X	X
	V2	0	0	1	0	X	X	X	X

Note

1. X = reserved.

17.2.2 SUBADDRESS 02

Table 12 Analog control 1 SA02

FUNCTION[1]	CONTROL BITS D2 TO D0		
	MODE 2	MODE 1	MODE 0
Mode 0: CVBS (automatic gain)	0	0	0
Mode 1: CVBS (automatic gain)	0	0	1
Mode 2: CVBS (automatic gain)	0	1	0
Mode 3: CVBS (automatic gain)	0	1	1
Mode 4: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	0
Mode 5: Y (automatic gain) + C (gain channel 2 fixed to GAI2 level)	1	0	1
Mode 6: Y (automatic gain) + C (gain channel 2 adapted to Y gain)	1	1	0
Mode 7: Y (automatic gain) + C (gain channel 2 adapted to Y gain)	1	1	1

Note

1. Mode select (see Figures 34 to 41).

Table 13 Analog control 1 SA 02, D5 to D3 (see Fig.15)

DECIMAL VALUE	UPDATE HYSTERESIS FOR 9-BIT GAIN	CONTROL BITS D5 TO D3		
		GUDL 2	GUDL 1	GUDL 0
0....	off	0	0	0
....7	±7 LSB	1	1	1

Table 14 Analog control

ANALOG FUNCTION SELECT FUSE	CONTROL BITS D7 AND D6	
	FUSE 1	FUSE 0
Amplifier plus anti-alias filter bypassed	0	0
	0	1
Amplifier active	1	0
Amplifier plus anti-alias filter active	1	1

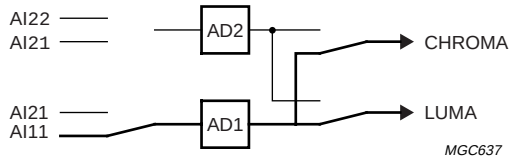


Fig.34 Mode 0; CVBS (automatic gain).

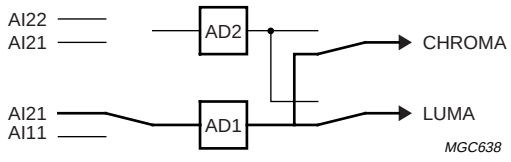


Fig.35 Mode 1; CVBS (automatic gain).

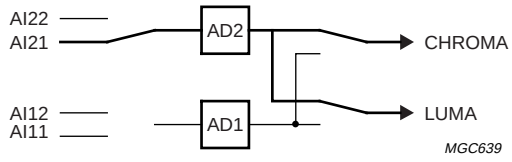


Fig.36 Mode 2; CVBS (automatic gain).

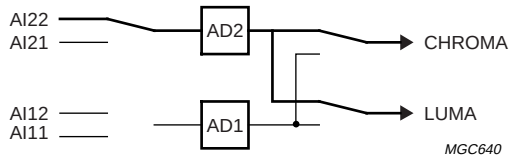


Fig.37 Mode 3; CVBS (automatic gain).

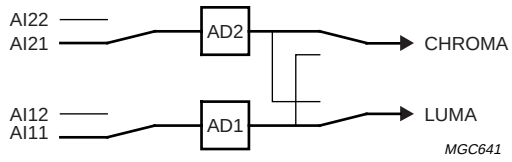


Fig.38 Mode 4 Y (automatic gain) + C (gain channel 2 fixed to GAI2 level).

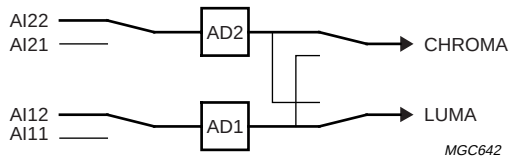


Fig.39 Mode 5 Y (automatic gain) + C (gain channel 2 fixed to GAI2 level).

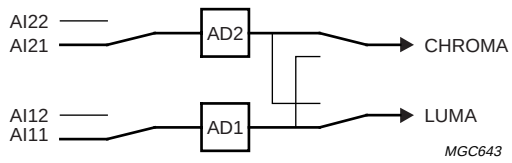


Fig.40 Mode 6 Y (automatic gain) + C (gain channel 2 adapted to Y gain).

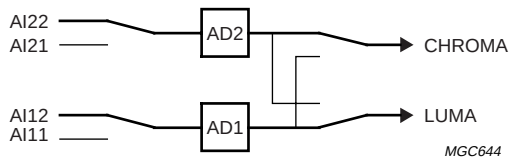


Fig.41 Mode 7 Y (automatic gain) + C (gain channel 2 adapted to Y gain).

17.2.3 SUBADDRESS 03

Table 15 Analog control 2 (AICO2) SA03

FUNCTION	LOGIC LEVEL	DATA BIT
Static gain control channel 1 (GAI18) (see SA04)		
Sign bit of gain control	see Table 16	D0
Static gain control channel 2 (GAI28) (see SA05)		
Sign bit of gain control	see Table 17	D1
Gain control fix (GAFIX)		
Automatic gain controlled by MODE 1 and MODE 0	0	D2
Gain control is user programmable via GAI1 + GAI2	1	D2
Automatic gain control integration (HOLDG)		
AGC active	0	D3
AGC integration hold (freeze)	1	D3
White peak off (WPOFF)		
White peak control active	0	D4
White peak off	1	D4
Vertical blanking select (VBSL)		
Long vertical blanking	0	D5
Short vertical blanking	1	D5
HL not reference select (HLNRS)		
Normal clamping by HL not	0	D6
Reference select by HL not	1	D6

17.2.4 SUBADDRESS 04

Table 16 Gain control analog (AIC03); static gain control channel 1 GAI1 SA 04, D7 to D0

DECIMAL VALUE	GAIN (dB)	SIGN BIT	CONTROL BITS D7 TO D0							
		GAI18	GAI17	GAI16	GAI15	GAI14	GAI13	GAI12	GAI11	GAI10
0....	–5.98	0	0	0	0	0	0	0	0	0
....255	0	0	1	1	1	1	1	1	1	1
256....	0	1	0	0	0	0	0	0	0	0
....511	5.98	1	1	1	1	1	1	1	1	1

17.2.5 SUBADDRESS 05

Table 17 Gain control analog (AIC04); static gain control channel 2 GAI2 SA 05, D7 to D0

DECIMAL VALUE	GAIN (dB)	SIGN BIT (SA 03, D1)	CONTROL BITS D7 to D0							
		GAI28	GAI27	GAI26	GAI25	GAI24	GAI23	GAI22	GAI21	GAI20
0....	–5.98	0	0	0	0	0	0	0	0	0
....255	0	0	1	1	1	1	1	1	1	1
256....	0	1	0	0	0	0	0	0	0	0
....511	5.98	1	1	1	1	1	1	1	1	1

17.2.6 SUBADDRESS 06

Table 18 Horizontal sync begin SA 06, D7 to D0

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSB7	HSB6	HSB5	HSB4	HSB3	HSB2	HSB1	HSB0
–128...–108	forbidden (outside available central counter range)							
–107...	1	0	0	1	0	1	0	1
...108	0	1	1	0	1	1	0	0
109...127	forbidden (outside available central counter range)							

17.2.7 SUBADDRESS 07

Table 19 Horizontal sync stop SA 07, D7 to D0

DELAY TIME (STEP SIZE = 8/LLC)	CONTROL BITS D7 to D0							
	HSS7	HSS6	HSS5	HSS4	HSS3	HSS2	HSS1	HSS0
–128...–108	forbidden (outside available central counter range)							
–107...	1	0	0	1	0	1	0	1
...108	0	1	1	0	1	1	0	0
109...127	forbidden (outside available central counter range)							

17.2.8 SUBADDRESS 08

Table 20 Sync control SA 08, D7 to D5, D3 to D0

FUNCTION	VNOI BITS	LOGIC LEVELS	DATA BITS
Vertical noise reduction (VNOI)			
Normal mode	VNOI1	0	D1
	VNOI0	0	D0
Searching mode	VNOI1	0	D1
	VNOI0	1	D0
Free running mode	VNOI1	1	D1
	VNOI0	0	D0
Vertical noise reduction bypassed	VNOI1	1	D1
	VNOI0	1	D0
Horizontal PLL (HPLL)			
PLL closed	HPLL	0	D2
PLL open, horizontal frequency fixed	HPLL	1	D2
TV/VTR mode select (VTRC)			
TV mode (recommended for poor quality TV signals only)	VTRC	0	D3
VTR mode (recommended as default setting)	VTRC	1	D3
Extended loop filter (EXFIL)			
Word width of the loop filter (LF2) amplification = 16-bit	EXFIL	0	D5
Word width of the loop filter (LF2) amplification = 14-bit	EXFIL	1	D5
Field selection (FSEL)			
50 Hz, 625 lines	FSEL	0	D6
60 Hz, 525 lines	FSEL	1	D6
Automatic field detection (AUFD)			
Field state directly controlled via FSEL	AUFD	0	D7
Automatic field detection	AUFD	1	D7

17.2.9 SUBADDRESS 09

Table 21 Luminance control SA 09, D7 to D0

FUNCTION	APER/BPSS BITS	LOGIC LEVELS	DATA BITS
Aperture factor (APER)			
Aperture factor = 0	APER1	0	D1
	APER0	0	D0
Aperture factor = 0.25	APER1	0	D1
	APER0	1	D0
Aperture factor = 0.5	APER1	1	D1
	APER0	0	D0
Aperture factor = 1.0	APER1	1	D1
	APER0	1	D0
Update time interval for AGC value (UPTCV)			
Horizontal update (once per line)	UPTCV	0	D2
Vertical update (once per field)	UPTCV	1	D2
Vertical blanking luminance bypass (VBLB)			
Active luminance processing	VBLB	0	D3
Luminance bypass during vertical blanking	VBLB	1	D3
Aperture band pass (centre frequency) (BPSS)			
Centre frequency = 4.1 MHz	BPSS1	0	D5
	BPSS0	0	D4
Centre frequency = 3.8 MHz; note 1	BPSS1	0	D5
	BPSS0	1	D4
Centre frequency = 2.6 MHz; note 1	BPSS1	1	D5
	BPSS0	0	D4
Centre frequency = 2.9 MHz; note 1	BPSS1	1	D5
	BPSS0	1	D4
Prefilter active (PREF)			
Bypassed	PREF	0	D6
Active	PREF	1	D6
Chrominance trap bypass (BYPS)			
Chrominance trap active; default for CVBS mode	BYPS	0	D7
Chrominance trap bypassed; default for S-Video mode	BYPS	1	D7

Note

1. Not to be used with bypassed chrominance trap.

17.2.10 SUBADDRESS 0A

Table 22 Luminance brightness control BRIG7 to BRIG0 SA 0A

OFFSET	CONTROL BITS D7 to D0							
	BRIG7	BRIG6	BRIG5	BRIG4	BRIG3	BRIG2	BRIG1	BRIG0
255 (bright)	1	1	1	1	1	1	1	1
128 (CCIR level)	1	0	0	0	0	0	0	0
0 (dark)	0	0	0	0	0	0	0	0

17.2.11 SUBADDRESS 0B

Table 23 Luminance contrast control CONT7 to CONT0 SA 0B

GAIN	CONTROL BITS D7 to D0							
	CONT7	CONT6	CONT5	CONT4	CONT3	CONT2	CONT1	CONT0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.109 (CCIR level)	0	1	0	0	0	1	1	1
1.0	0	1	0	0	0	0	0	0
0 (luminance off)	0	0	0	0	0	0	0	0
−1 (inverse luminance)	1	1	0	0	0	0	0	0
−2 (inverse luminance)	1	0	0	0	0	0	0	0

17.2.12 SUBADDRESS 0C

Table 24 Chrominance saturation control SATN7 to SATN0 SA 0C

GAIN	CONTROL BITS D7 to D0							
	SATN7	SATN6	SATN5	SATN4	SATN3	SATN2	SATN1	SATN0
1.999 (maximum)	0	1	1	1	1	1	1	1
1.0 (CCIR level)	0	1	0	0	0	0	0	0
0 (colour off)	0	0	0	0	0	0	0	0
−1 (inverse chrominance)	1	1	0	0	0	0	0	0
−2 (inverse chrominance)	1	0	0	0	0	0	0	0

17.2.13 SUBADDRESS 0D

Table 25 Chrominance hue control HUEC7 to HUEC0 SA 0D

HUE PHASE (DEG)	CONTROL BITS D7 to D0							
	HUEC7	HUEC6	HUEC5	HUEC4	HUEC3	HUEC2	HUEC1	HUEC0
+178.6....	0	1	1	1	1	1	1	1
....0....	0	0	0	0	0	0	0	0
....–180	1	0	0	0	0	0	0	0

17.2.14 SUBADDRESS 0E

Table 26 Chrominance control SA 0E

FUNCTION	CHBW/CSTD BITS	LOGIC LEVELS	DATA BITS
Chroma bandwidth (CHBW0 and CHBW1)			
Small bandwidth (≈ 620 kHz)	CHBW1	0	D1
	CHBW0	0	D0
Nominal bandwidth (≈ 800 kHz)	CHBW1	0	D1
	CHBW0	1	D0
Medium bandwidth (≈ 920 kHz)	CHBW1	1	D1
	CHBW0	0	D0
Wide bandwidth (≈ 1000 kHz)	CHBW1	1	D1
	CHBW0	1	D0
Fast colour time constant (FCTC)			
Nominal time constant	FCTC	0	D2
Fast time constant	FCTC	1	D2
Disable chrominance comb filter (DCCF)			
Chrominance comb filter on (during VREF = 1) (see Figs 25 and 26)	DCCF	0	D3
Chrominance comb filter off	DCCF	1	D3
Colour standard (CSTD0 to CSTD2); logic levels 100, 110 and 111 are reserved, do not use			
Colour standard control automatic switching between PAL BGHI and NTSC M (NTSC-Japan with special level adjustment; luminance brightness subaddress 0A = 95H, luminance contrast subaddress 0BH = 48H)	CSTD2	0	D6
	CSTD1	0	D5
	CSTD0	0	D4
Colour standard control automatic switching between NTSC 4.43 (50 Hz) and PAL 4.43 (60 Hz)	CSTD2	0	D6
	CSTD1	0	D5
	CSTD0	1	D4
Colour standard control automatic switching between PAL N and NTSC 4.43 (60 Hz)	CSTD2	0	D6
	CSTD1	1	D5
	CSTD0	0	D4
Colour standard control automatic switching between NTSC N and PAL M	CSTD2	0	D6
	CSTD1	1	D5
	CSTD0	1	D4
Colour standard control automatic switching between SECAM and PAL 4.43 (60 Hz)	CSTD2	1	D6
	CSTD1	0	D5
	CSTD0	1	D4
Clear DTO (CDTO)			
Disabled	CDTO	0	D7
Every time CDTO is set, the internal subcarrier DTO phase is reset to 0° and the RTCO output generates a logic 0 at time slot 68 (see RTCO description Fig.21). So an identical subcarrier phase can be generated by an external device (e.g. an encoder).	CDTO	1	D7

17.2.15 SUBADDRESS 10

Table 27 Format/delay control SA 10

LUMINANCE DELAY COMPENSATION (STEPS IN 2/LLC)	CONTROL BITS D2 to D0		
	YDEL2	YDEL1	YDEL0
–4...	1	0	0
...0...	0	0	0
...3	0	1	1

Table 28 VREF pulse position and length VRLN SA 10 (D3)

VRLN	VREF at 60 Hz 525 LINES(2)				VREF at 50 Hz 625 LINES(2)			
	0		1		0		1	
Length	240		242		286		288	
Line number	first	last	first	last	first	last	first	last
Field 1(1)	19 (22)	258 (261)	18 (21)	259 (262)	24	309	23	310
Field 2(1)	282 (285)	521 (524)	281 (284)	522 (525)	337	622	336	623

Notes

1. The numbers given in parenthesis refer to CCIR line counting.
2. Additional VREF positions can be achieved via I^{2}C-bus bits VCTR1 and VCTR0 (see Fig.10).

Table 29 Fine position of HS HDEL0 and HDEL1 SA 10

FINE POSITION OF HS WITH A STEP SIZE OF 2/LLC	CONTROL BITS D5 and D4	
	HDEL1	HDEL0
0	0	0
1	0	1
2	1	0
3	1	1

Table 30 Output format selection OFTS0 and OFTS1 SA 10

FORMATS	CONTROL BITS D7 and D6	
	OFTS1	OFTS0
RGB (5, 6, 5), RGB (8, 8, 8) (dependent on control bit RGB888) see Table 32	0	0
YUV 422 16 bits	0	1
YUV 411 12 bits	1	0
YUV CCIR-656 8 bits	1	1

17.2.16 SUBADDRESS 11

Table 31 Output control 1 SA 11

FUNCTION	BITS	LOGIC LEVELS	DATA BIT
Colour on (COLO)			
Automatic colour killer	COLO	0	D0
Colour forced on	COLO	1	D0
Decoder VIP bypassed (VIPB)			
DMSD data to YUV output	VIPB	0	D1
ADC data to YUV output; dependent on mode settings	VIPB	1	D1
Output enable horizontal/vertical sync (OEHV)			
HS, HREF, VREF and VS high-impedance inputs	OEHV	0	D2
Outputs HS, HREF, VREF and VS active	OEHV	1	D2
Output enable YUV data (OEYC)			
VPO-bus high-impedance inputs	OEYC	0	D3
Output VPO-bus active	OEYC	1	D3
Inverse composite blank (COMPO)			
VREF is vertical reference	COMPO	0	D4
VREF is inverse composite blank	COMPO	1	D4
$\overline{\text{FEI}}$ control (FECO)			
$\overline{\text{FEI}}$ sampling at CREF = LOW (SAA7110 compatible; (see Fig.20)	FECO	0	D5
$\overline{\text{FEI}}$ sampling at CREF = HIGH	FECO	1	D5
CM99 compatibility to SAA7199 (CM99)			
Default value	CM99	0	D6
To be set if SAA7199 (digital encoder) is used for re-encoding in conjunction with RTCO	CM99	1	D6
General purpose switch (GPSW)			
Switches directly pin 64 GPSW	GPSW	0	D7
	GPSW	1	D7

17.2.17 SUBADDRESS 12

Table 32 Output control 2 SA 12, D7 to D6, D4 to D0

FUNCTION	AOSL BITS	LOGIC LEVELS	DATA BITS
Analog test select (AOSL)			
AOUT connected to internal test point 1	AOSL1	0	D1
	AOSL0	0	D0
AOUT connected to input AD1	AOSL1	0	D1
	AOSL0	1	D0
AOUT connected to input AD2	AOSL1	1	D1
	AOSL0	0	D0
AOUT connected to internal test point 2	AOSL1	1	D1
	AOSL0	1	D0
Dithering (noise shaping) control (DIT)			
Dithering off	DIT	0	D2
Dithering on	DIT	1	D2
RGB output format selection (RGB888)			
RGB (5, 6, 5)	RGB888	0	D3
RGB (8, 8, 8)	RGB888	1	D3
Chrominance interpolation filter function (CBR)			
Cubic interpolation (default)	CBR	0	D4
Linear interpolation (lower bandwidth)	CBR	1	D4
3-state control VPO7 to VPO0 (TCLO)			
VPO7 to VPO0 depends on OEYC, $\overline{\text{FEI}}$ only (default)	TCLO	0	D5
VPO7 to VPO0 in 3-state [and OFTS (1 : 0) = 3]	TCLO	1	D5
Real time outputs mode select (RTSE0)			
ODD switched to output pin 40	RTSE0	0	D6
VL switched to output pin 40	RTSE0	1	D6
Real time outputs mode select (RTSE1)			
PLIN switched to output pin 39	RTSE1	0	D7
HL switched to output pin 39	RTSE1	1	D7

17.2.18 SUBADDRESS 13

Table 33 Output control 3 SA 13

FUNCTION	BITS	LOGIC LEVELS	DATA BITS
Bypass control LOW for VPO7 to VPO0			
No bypass	BCLO1	0	D1
	BCLO0	0	D0
Permanent bypass	BCLO1	0	D1
	BCLO0	1	D0
Bypass controlled by V_GATE	BCLO1	1	D1
	BCLO0	0	D0
Bypass controlled by delayed V_GATE	BCLO1	1	D1
	BCLO0	1	D0
Bypass control HIGH for VPO15 to VPO8			
No bypass	BCHI1	0	D3
	BCHI0	0	D2
Permanent bypass	BCHI1	0	D3
	BCHI0	1	D2
Bypass controlled by V_GATE	BCHI1	1	D3
	BCHI0	0	D2
Bypass controlled by delayed V_GATE	BCHI1	1	D3
	BCHI0	1	D2
Clock Reference Output Control			
CREF is independent of VREF	CCTR1	0	D5
	CCTR0	0	D4
CREF is LOW if VREF = 0	CCTR1	0	D5
	CCTR0	1	D4
CREF is HIGH if VREF = 0	CCTR1	1	D5
	CCTR0	0	D4
CREF always = 1	CCTR1	1	D5
	CCTR0	1	D4
Vertical Reference Output Control (VREF)			
Internal VREF	VCTR1	0	D7
	VCTR0	0	D6
VREF_CCIR	VCTR1	0	D7
	VCTR0	1	D6
Programmable V_GATE	VCTR1	1	D7
	VCTR0	0	D6
Delayed programmable V_GATE	VCTR1	1	D7
	VCTR0	1	D6

17.2.19 SUBADDRESS 15

Table 34 Start of decoded data on VPO-port SA 15; note 1

FIELD		Frame line(2) counting	Decimal value	MSB (SA 17, D0)	CONTROL BITS D7 to D0							
				VSTA8	VSTA 7	VSTA 6	VSTA 5	VSTA 4	VSTA 3	VSTA 2	VSTA 1	VSTA 0
50 Hz	1st	1	312	1	0	0	1	1	1	0	0	0
	2nd	314										
	1st	2	0....	0	0	0	0	0	0	0	0	0
	2nd	315										
	1st	312	310	1	0	0	1	1	0	1	1	1
	2nd	625										
60 Hz	1st	1 (4)	262	1	0	0	0	0	0	1	1	0
	2nd	264 (267)										
	1st	2 (5)	0....	0	0	0	0	0	0	0	0	0
	2nd	265 (268)										
	1st	262 (265)	260	1	0	0	0	0	0	1	0	1
	2nd	525 (3)										

Notes

1. Start of decoded data on VPO-port (end of bypassed region; start of VREF if selected by VCTR1 and VCTR0; see Figs 9 and 11).
2. Line numbers in brackets refer to CCIR line counting.

17.2.20 SUBADDRESS 16

Table 35 Stop of decoded data on VPO-port SA 16; note 1

FIELD		Frame line(2) counting	Decimal value	MSB (SA 17, D0)	CONTROL BITS D7 to D0							
				VSTO8	VSTO 7	VSTO 6	VSTO 5	VSTO 4	VSTO 3	VSTO 2	VSTO 1	VSTO 0
50 Hz	1st	1	312	1	0	0	1	1	1	0	0	0
	2nd	314										
	1st	2	0....	0	0	0	0	0	0	0	0	0
	2nd	315										
	1st	312	310	1	0	0	1	1	0	1	1	1
	2nd	625										
60 Hz	1st	1 (4)	262	1	0	0	0	0	0	1	1	0
	2nd	264 (267)										
	1st	2 (5)	0....	0	0	0	0	0	0	0	0	0
	2nd	265 (268)										
	1st	262 (265)	260	1	0	0	0	0	0	1	0	1
	2nd	525 (3)										

Notes

1. Stop of decoded data on VPO-port (begin of bypassed region; stop of VREF if selected by VCTR1 and VCTR0; see Figs 9 and 11).
2. Line numbers in brackets refer to CCIR line counting.

17.2.21 SUBADDRESS 17

Table 36 Sign bits of the VBI-data stream control

FUNCTION	LOGIC LEVELS	CONTROL BITS
VBI-data stream start (VSTA8); see SA 15		
Sign bit VBI-data stream start	see Table 34	D0
VBI-data stream stop (VSTA8); see SA 16		
Sign bit VBI-data stream stop	see Table 35	D1

17.2.22 SUBADDRESS 1A (READ-ONLY REGISTER)

Table 37 Line-21 text slicer status SA 1A, D3 to D0

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
F1RDY	new data on field 1 has been acquired (for asynchronous reading); active HIGH	D0
F1VAL	Line-21 of field 1 carries valid data; active HIGH	D1
F2RDY	new data on field 2 has been acquired (for asynchronous reading); active HIGH	D2
F2VAL	Line-21 of field 2 carries valid data; active HIGH	D3

17.2.23 SUBADDRESS 1B (READ-ONLY REGISTER)

Table 38 First decoded data byte of the text slicer SA 1B

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
BYTE1 (6 to 0)	data bit 6 to 0 of first data byte	D6 to D0
P1	parity error flag bit; bit goes HIGH when a parity error has occurred	D7

17.2.24 SUBADDRESS 1C (READ-ONLY REGISTER)

Table 39 Second decoded data byte of the text slicer SA 1C

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
BYTE2 (6 to 0)	data bit 6 to 0 of second data byte	D6 to D0
P2	parity error flag bit; bit goes HIGH when a parity error has occurred	D7

17.2.25 SUBADDRESS 1F (READ-ONLY REGISTER)

Table 40 Status byte SA 1F

I²C-BUS CONTROL BITS	FUNCTION	DATA BIT
CODE	colour signal in accordance with selected standard has been detected; active HIGH	D0
SLTCA	slow time constant active in WIPA-mode; active HIGH	D1
WIPA	white peak loop is activated; active HIGH	D2
GLIMB	gain value for active luminance channel is limited [min (bottom)]; active HIGH	D3
GLIMT	gain value for active luminance channel is limited [max (top)]; active HIGH	D4
FIDT	identification bit for detected field frequency; LOW = 50 Hz, HIGH = 60 Hz	D5
HLCK	status bit for locked horizontal frequency; LOW = locked, HIGH = unlocked	D6
STTC	status bit for horizontal phase loop; LOW = TV time-constant, HIGH = VTR time-constant	D7

18 FILTER CURVES

18.1 Anti-alias filter curve

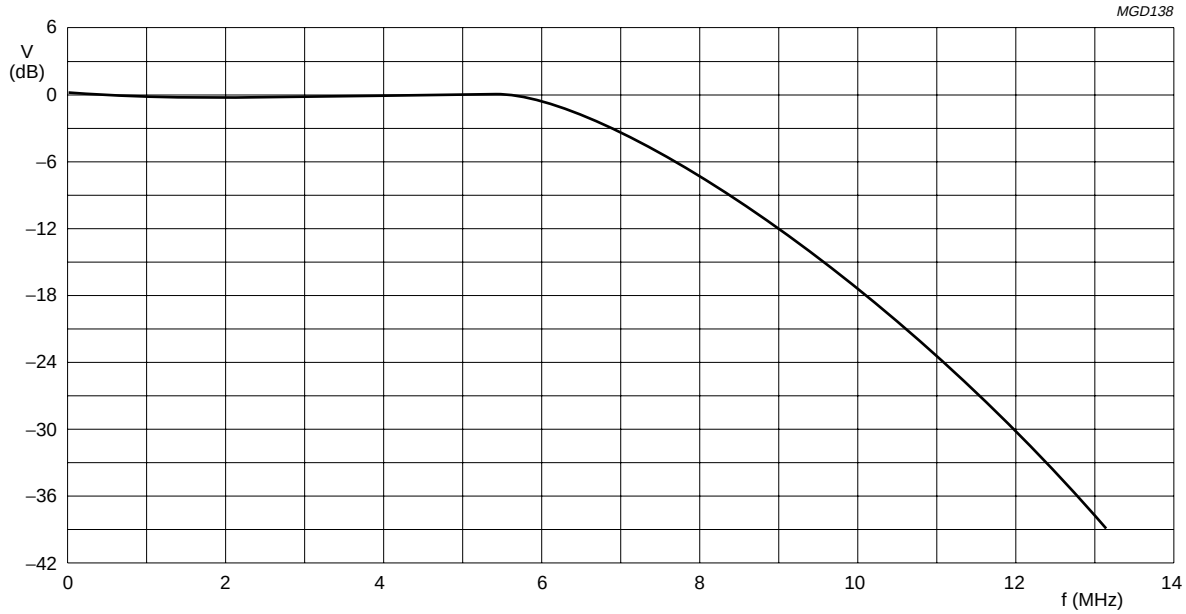


Fig.42 Anti-alias filter.

18.2 TUF-block filter curve

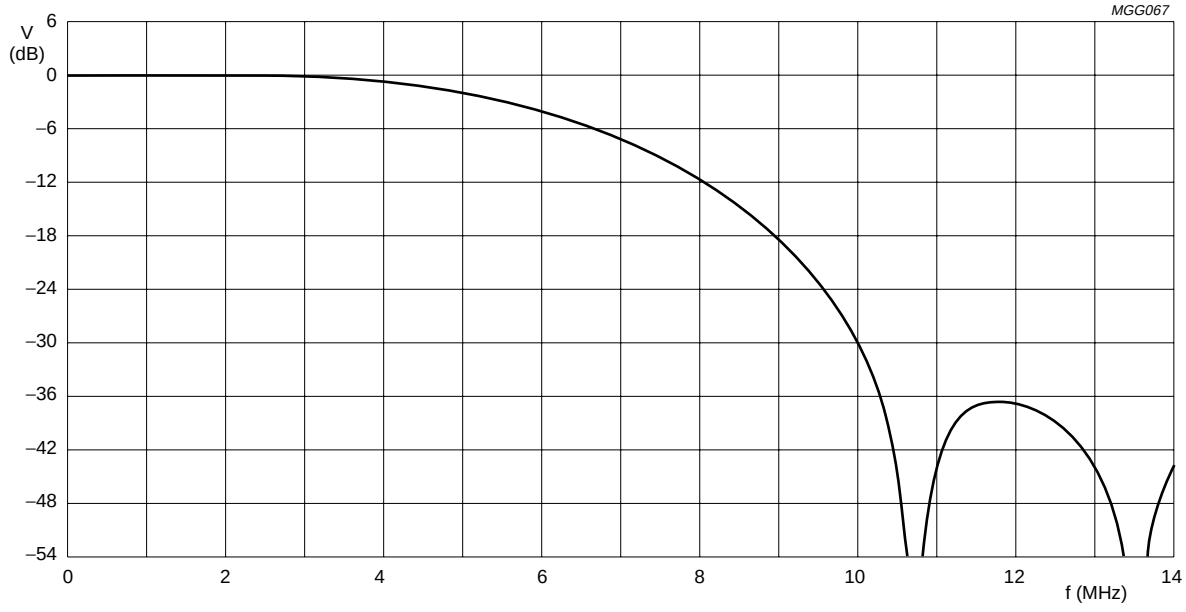
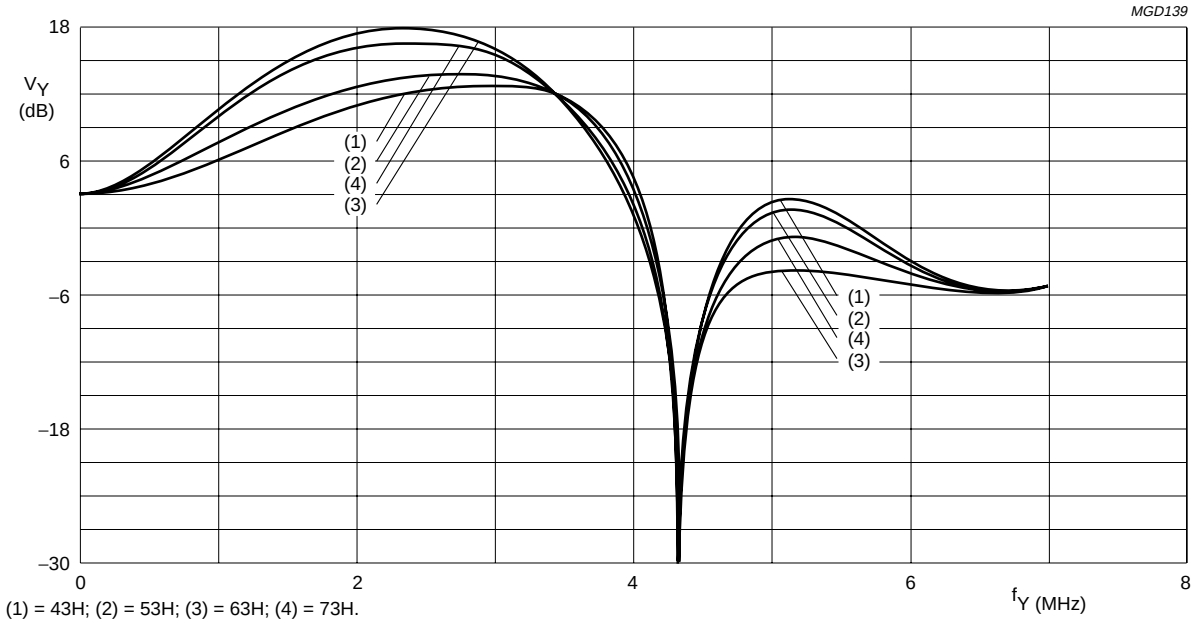


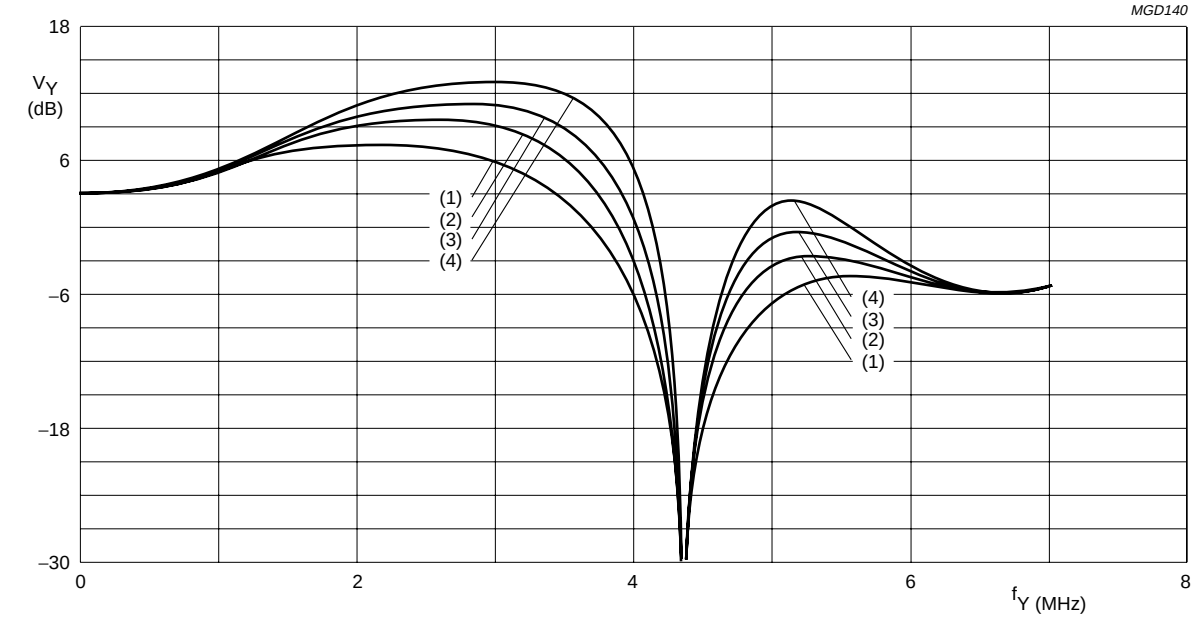
Fig.43 Interpolation filter for the upsampled CVBS-signal.

18.3 Luminance filter curves



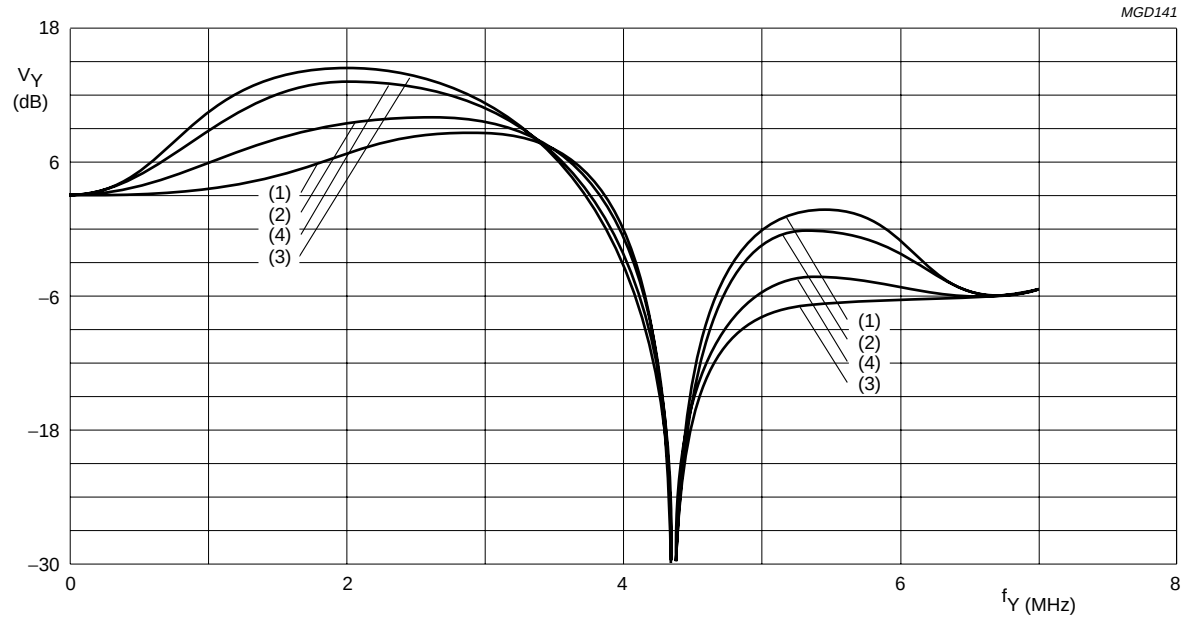
(1) = 43H; (2) = 53H; (3) = 63H; (4) = 73H.

Fig.44 Luminance control SA 09H, 4.43 MHz Trap/CVBS mode, prefilter on, different aperture bandpass centre frequencies.



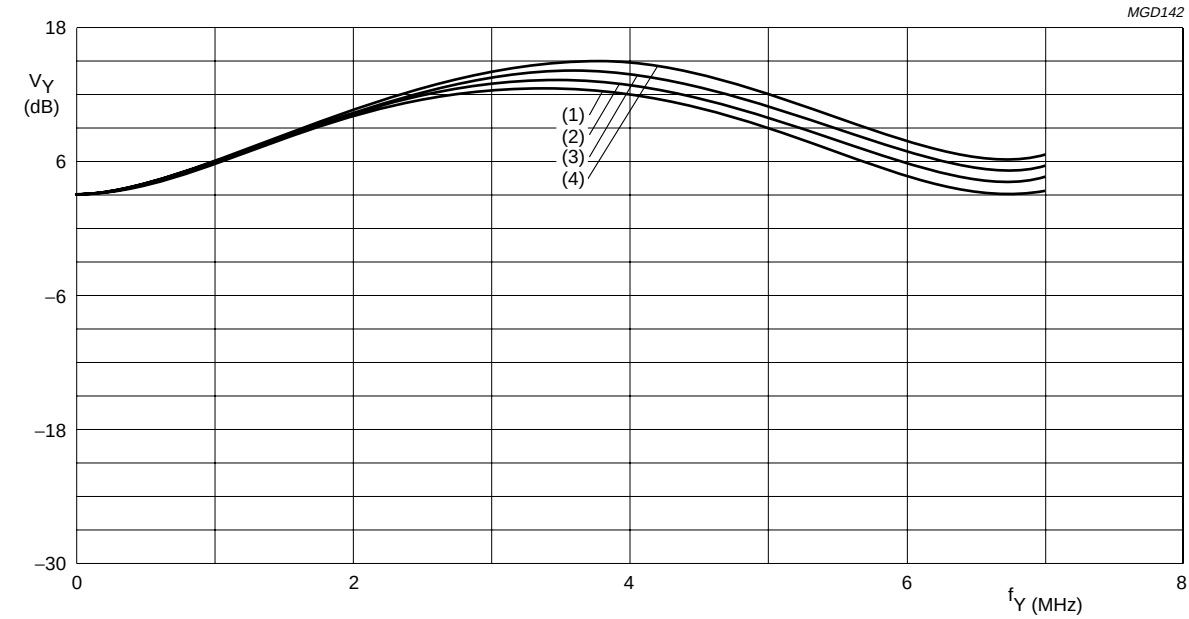
(1) = 40H; (2) = 41H; (3) = 42H; (4) = 43H.

Fig.45 Luminance control SA 09H, 4.43 MHz Trap/CVBS mode, prefilter on, different aperture factors.



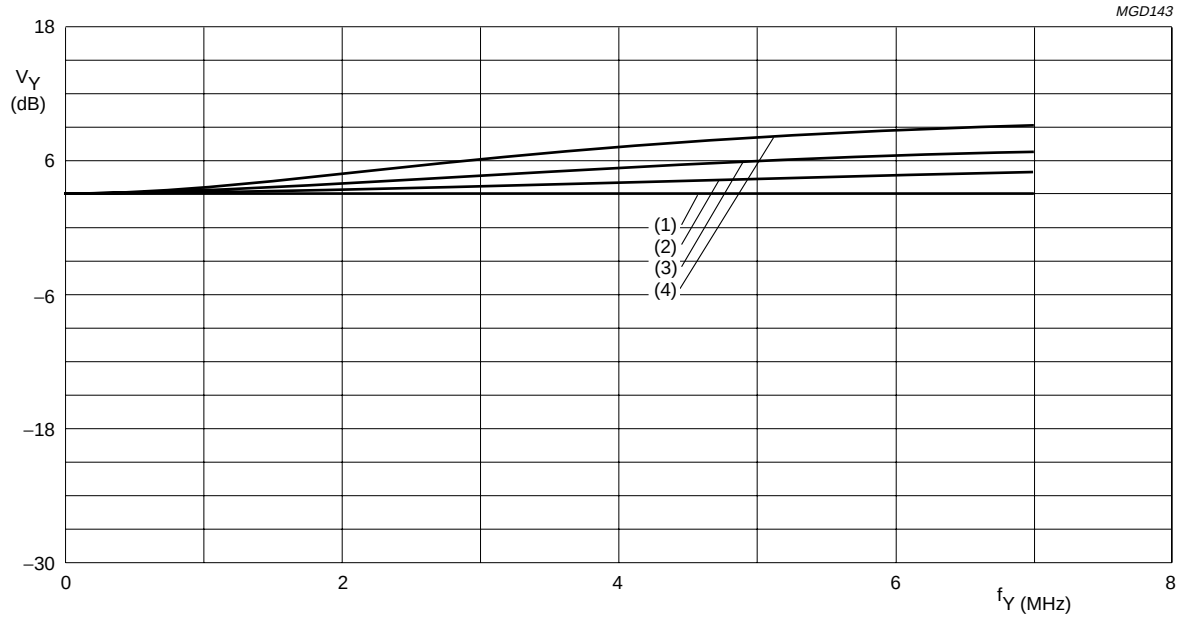
(1) = 03H; (2) = 13H; (3) = 23H; (4) = 33H.

Fig.46 Luminance control SA 09H, 4.43 MHz Trap/CVBS mode, prefilter off, different aperture band-pass centre frequencies.



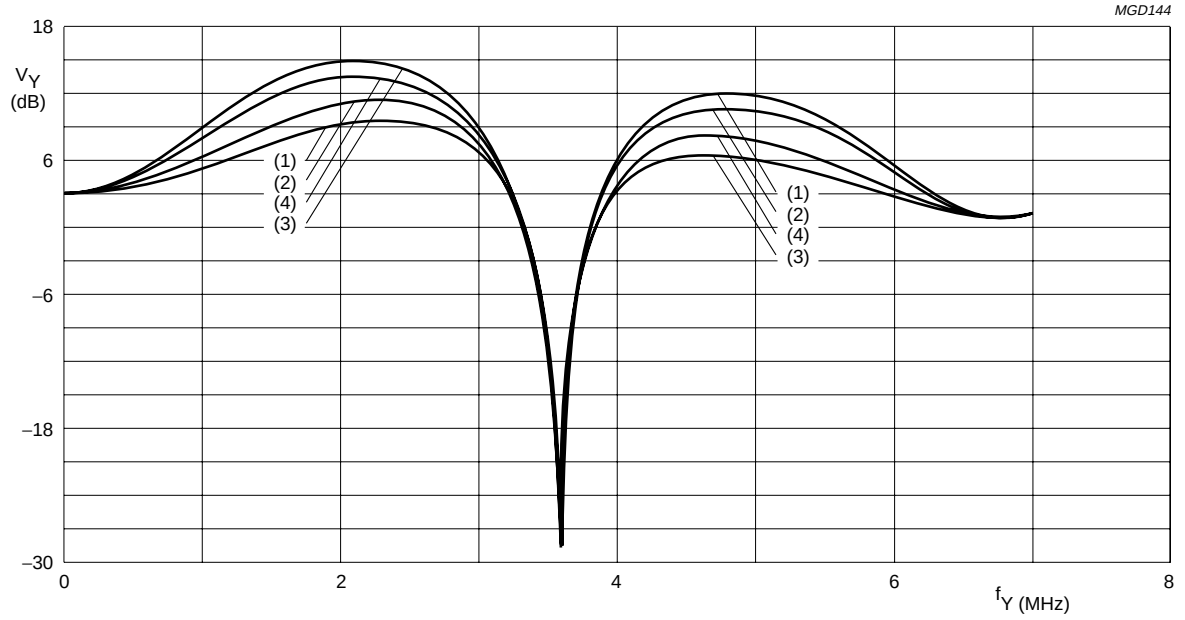
(1) = C0H; (2) = C1H; (3) = C2H; (4) = C3H.

Fig.47 Luminance control SA 09H, Y/C mode, prefilter on, different aperture factors.



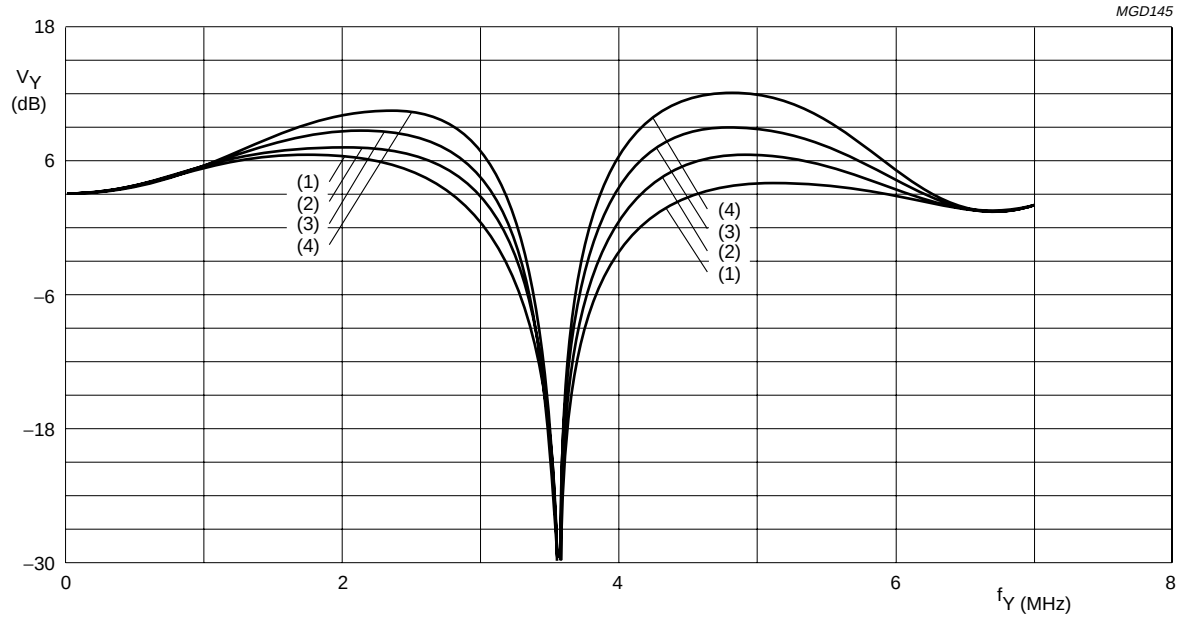
(1) = 80H; (2) = 81H; (3) = 82H; (4) = 83H.

Fig.48 Luminance control SA 09H, Y/C mode, prefilter off, different aperture factors.



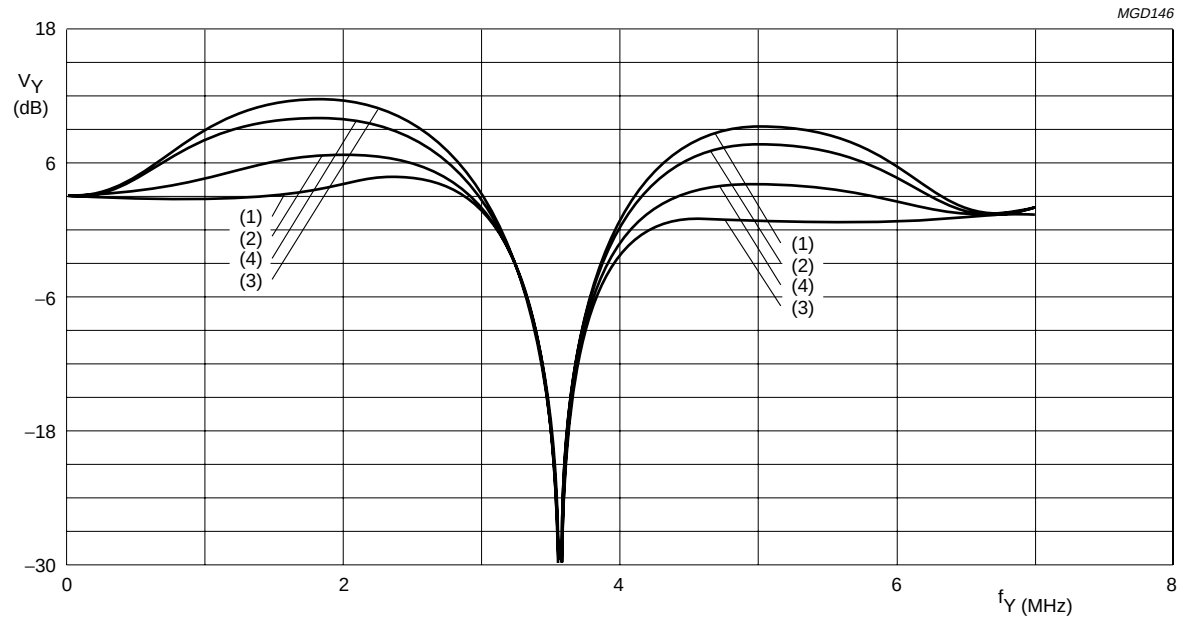
(1) = 43H; (2) = 53H; (3) = 63H; (4) = 73H.

Fig.49 Luminance control SA 09H, 3.58 MHz Trap/CVBS mode, prefilter on, different aperture band-pass centre frequencies.



(1) = 40H; (2) = 41H; (3) = 42H; (4) = 43H.

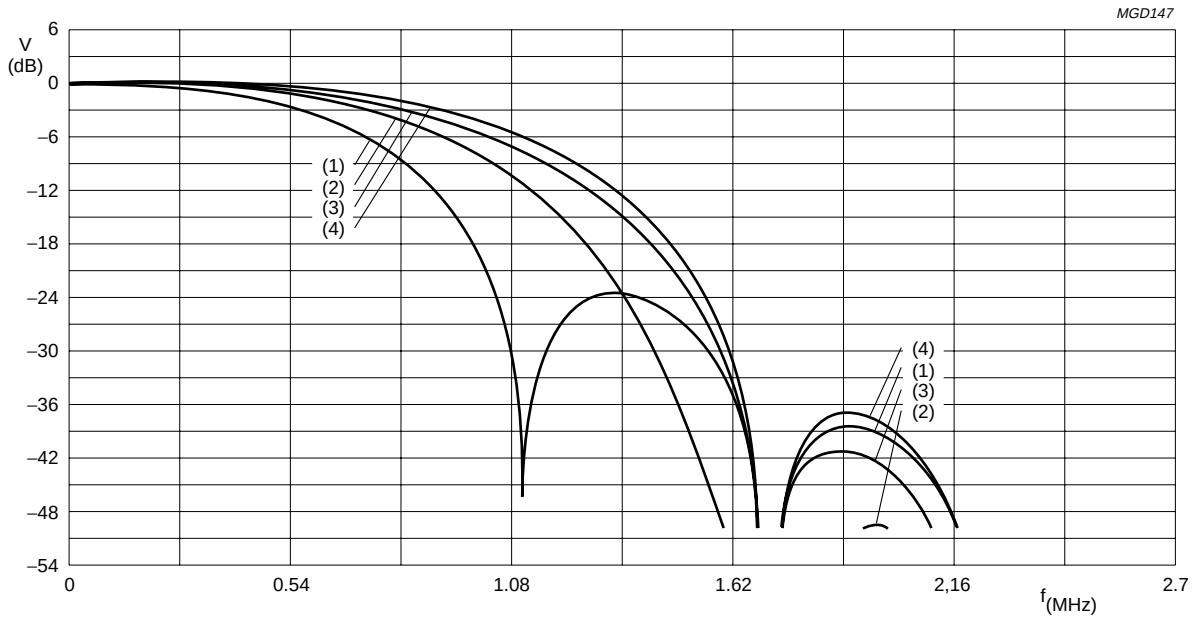
Fig.50 Luminance control SA 09H, 3.58 MHz Trap/CVBS mode, prefilter on, different aperture factors.



(1) = 03H; (2) = 13H; (3) = 23H; (4) = 33H.

Fig.51 Luminance control SA 09H, 3.58 MHz Trap/CVBS mode, prefilter off, different aperture band-pass centre frequencies.

18.4 Chrominance filter curves



Transfer characteristics of the chrominance low-pass dependent on CHBW[1 : 0] settings.
(1) CHBW [1 : 0] = 00; (2) CHBW [1 : 0] = 01; (3) CHBW [1 : 0] = 10; (4) CHBW [1 : 0] = 11.

Fig.52 Chrominance filter.

19 I²C-BUS START SET-UP

- The given values force the following behaviour of the SAA7111A:
  - the analog input AI11 expects a signal in CVBS format; analog anti-alias filter active
  - automatic field detection
  - YUV 4 : 2 : 2 16-bit output format enabled
  - outputs HS, HREF, VREF and VS active
  - contrast, brightness and saturation control in accordance with CCIR standards
  - chrominance processing with nominal bandwidth (800 kHz).

Table 41 I²C-bus start set-up values

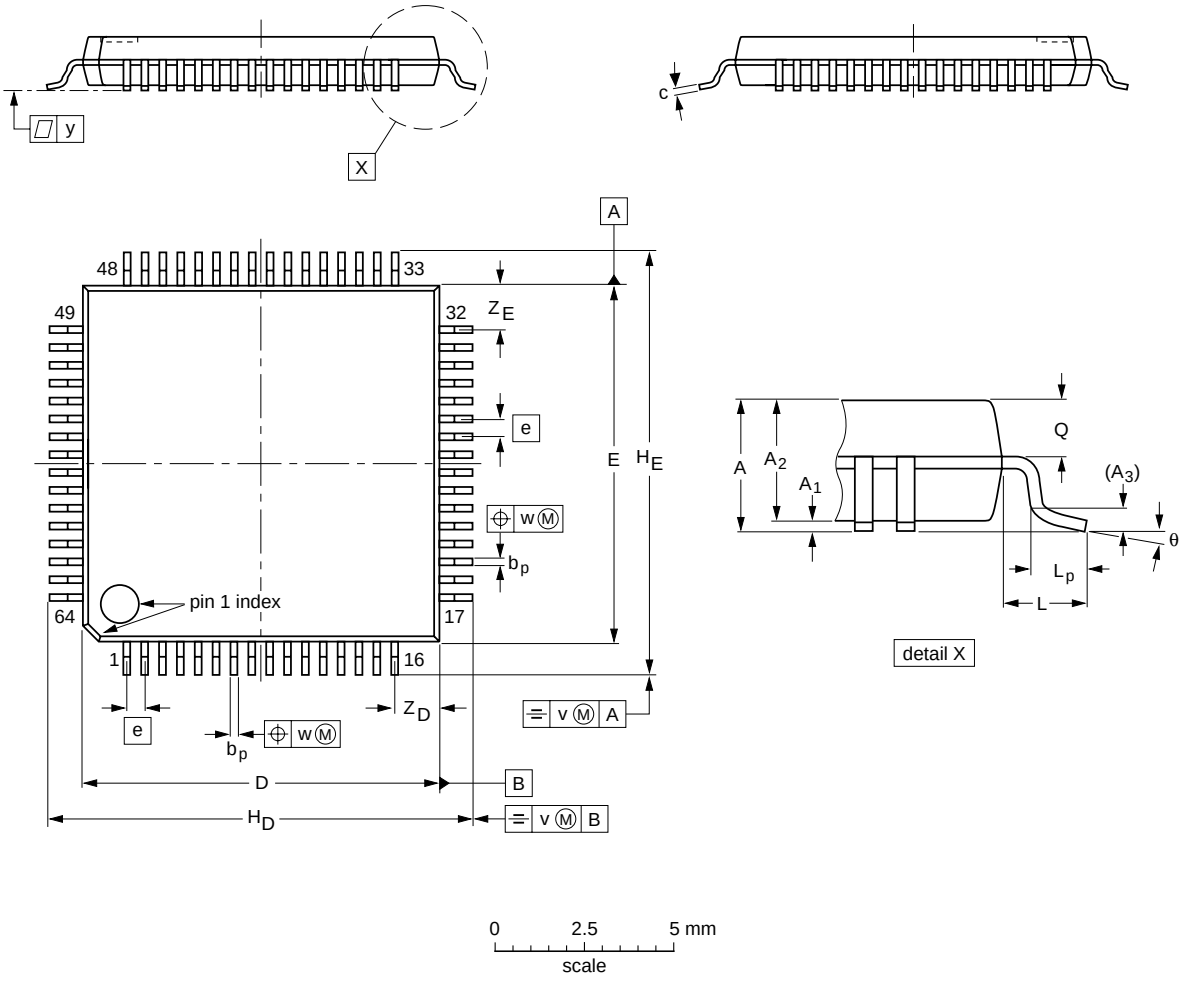
SUB (HEX)	FUNCTION	NAME[1]	VALUES (BIN)								(HEX)
			7	6	5	4	3	2	1	0	START
00	chip version	ID07 to ID00; see Table 9	read only								
01	reserved		0	0	0	0	0	0	0	0	00
02	analog input control 1	FUSE1 and FUSE0, GUDL2 to GUDL0, MODE2 to MODE0	1	1	0	0	0	0	0	0	C0
03	analog input control 2	X, HLNRS, VBSL, WPOFF, HOLDG, GAFIX, GAI28, GAI18	0	0	1	0	0	0	1	1	23
04	analog input control 3	GAI17 to GAI10	0	0	0	0	0	0	0	0	00
05	analog input control 4	GAI27 to GAI20	0	0	0	0	0	0	0	0	00
06	horizontal sync start	HSB7 to HSB0	1	1	1	0	1	0	1	1	EB
07	horizontal sync stop	HSS7 to HSS0	1	1	1	0	0	0	0	0	E0
08	sync control	AUFD, FSEL, EXFIL, X, VTRC, HPLL, VNOI1 and VNOI0	1	0	0	0	1	0	0	0	88
09	luminance control	BYPS, PREF, BPSS1 and BPSS0, VBLB, UPTCV, APER1 and APER0	0	0	0	0	0	0	0	1	01
0A	luminance brightness	BRIG7 to BRIG0	1	0	0	0	0	0	0	0	80
0B	luminance contrast	CONT7 to CONT0	0	1	0	0	0	1	1	1	47
0C	chrominance saturation	SATN7 to SATN0	0	1	0	0	0	0	0	0	40
0D	chroma hue control	HUEC7 to HUEC0	0	0	0	0	0	0	0	0	00
0E	chrominance control	CDTO, CSTD2 to CSTD0, DCCF, FCTC, CHBW1 and CHBW0	0	0	0	0	0	0	0	1	01
0F	reserved		0	0	0	0	0	0	0	0	00
10	format/delay control	OFTS1 and OFTS0, YDEL2 to YDEL0 HDEL1 and HDEL0, VRLN	0	1	0	0	0	0	0	0	40
11	output control 1	GPSW, CM99, FECO, COMPO, OEYC, OEHV, VIPB, COLO	0	0	0	1	1	1	0	0	1C
12	output control 2	RTSE1 and RTSE0, TCLO, CBR, RGB888 DIT, AOSL1 and AOSL0	0	0	0	0	0	0	0	1	01
13	output control 3	CCTR1 and CCTR0, BCHI1 and BCHI0, BCLO1 and BCLO0, VCTR1 and VCTR0	0	0	0	0	0	0	0	0	00
14	reserved		0	0	0	0	0	0	0	0	00
15	VBI-data stream start	VSTA7 to VSTA0	0	0	0	0	0	0	0	0	00
16	VBI-data stream stop	VSTO7 to VSTO0	0	0	0	0	0	0	0	0	00
17	MSBs for VBI control	X, X, X, X, X, X, VSTO8, VSTA8	0	0	0	0	0	0	0	0	00
18-19	reserved		0	0	0	0	0	0	0	0	00
1A	text slicer status	0, 0, 0, 0, F2VAL, F2RDY, F1VAL, F1RDY	read only register								
1B	decoded bytes of the text slicer	P1, BYTE1(6 to 0)									
1C		P2, BYTE2(6 to 0)									
1D-1E	reserved		0	0	0	0	0	0	0	0	00
1F	status byte	STTC, HLCK, FIDT, GLIMT, GLIMB, WIPA, SLTCA, CODE	read only register								

Note

1. All X values must be set to LOW.

20 PACKAGE OUTLINES

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

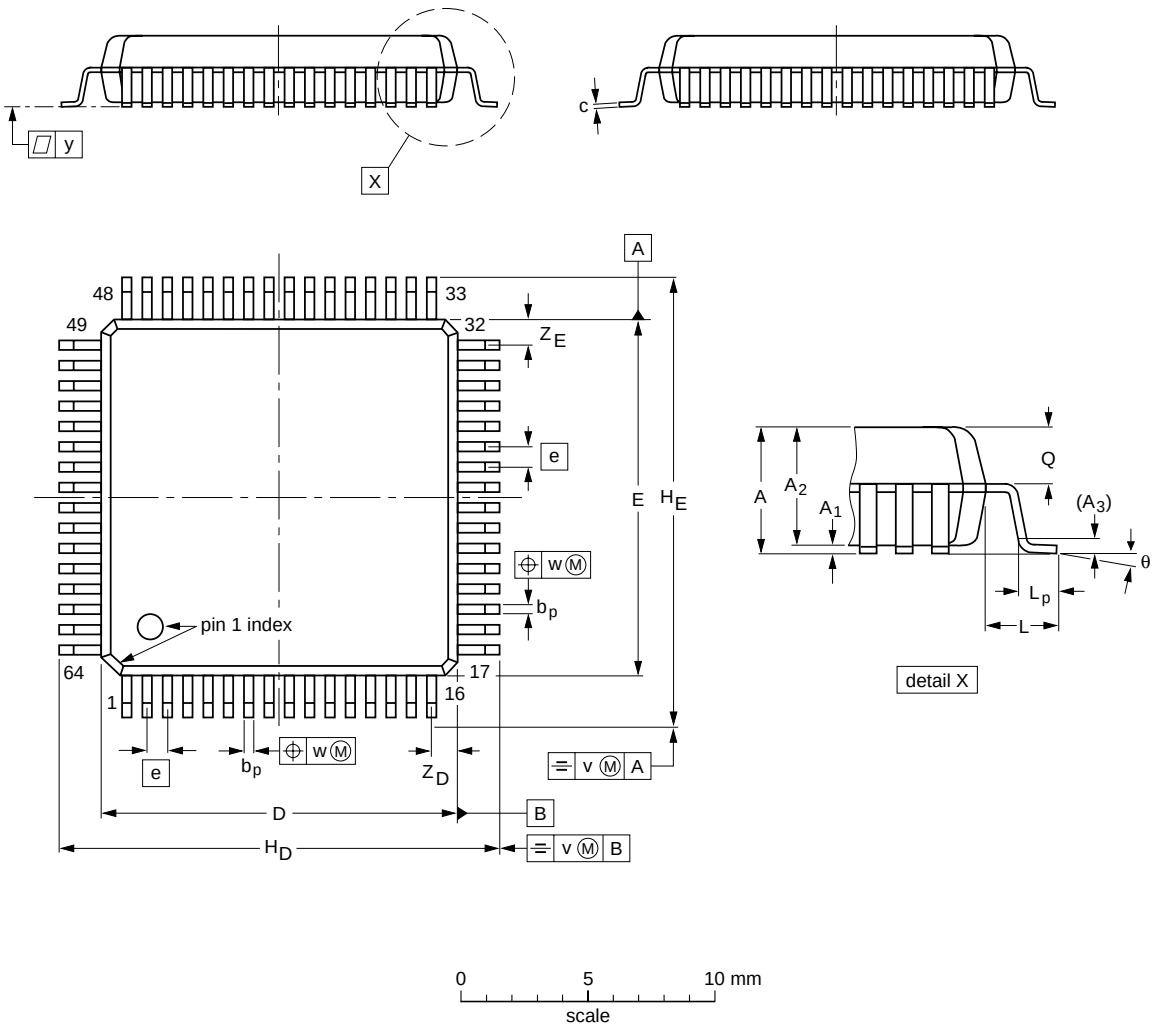
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-12-19

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

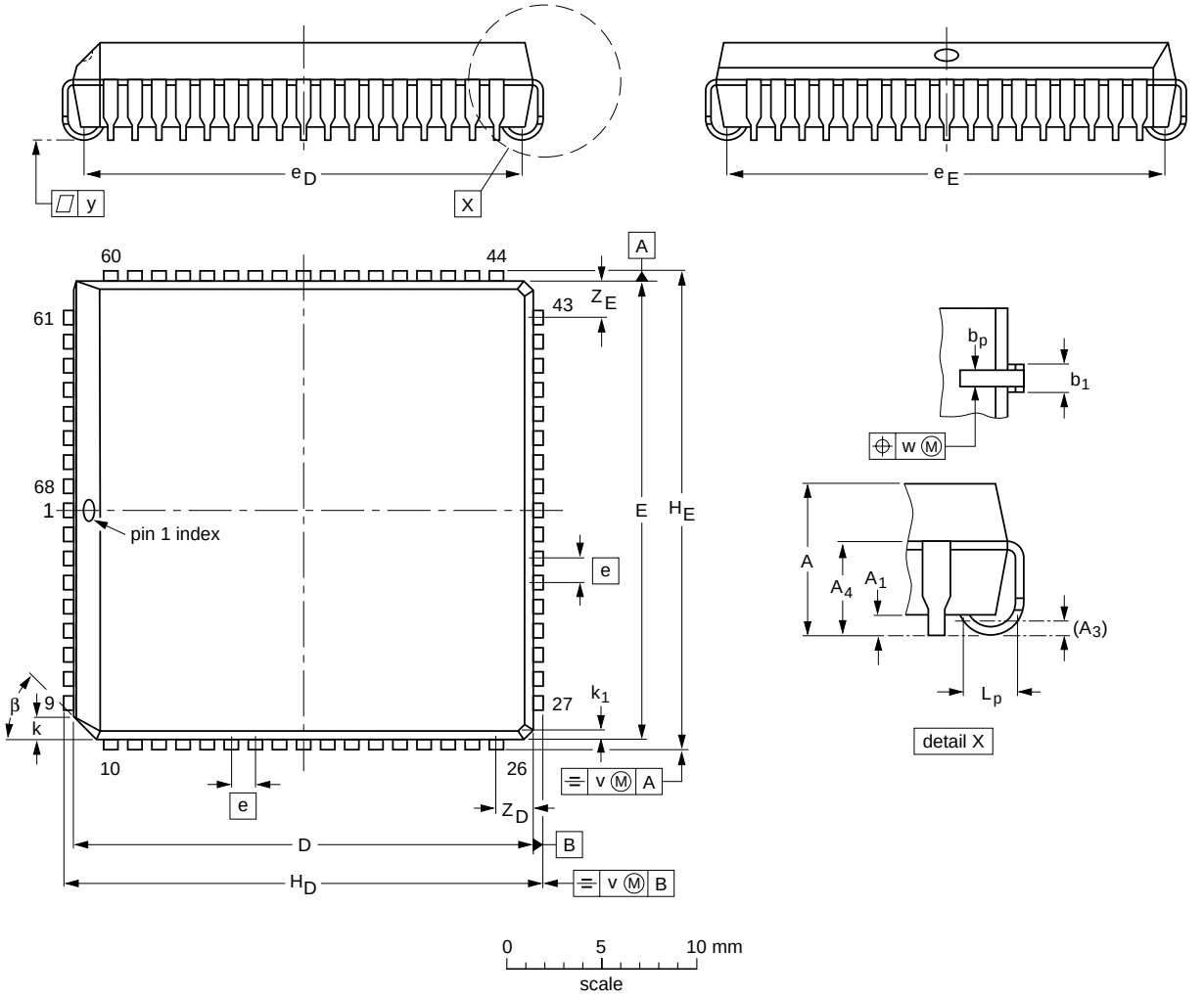
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	1.4 1.1	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1		MS-022				~~94-06-22~~ 96-05-21

PLCC68: plastic leaded chip carrier; 68 leads **SOT188-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.30	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.13	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-2	112E10	MO-047AC				~~92-11-17~~ 95-03-11

21 SOLDERING

21.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

21.2 Reflow soldering

Reflow soldering techniques are suitable for all PLCC and QFP packages.

The choice of heating method may be influenced by larger PLCC or QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

21.3 Wave soldering

21.3.1 PLCC

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

21.3.2 QFP

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

21.3.3 METHOD (PLCC AND QFP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

21.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

22 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

23 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

24 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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